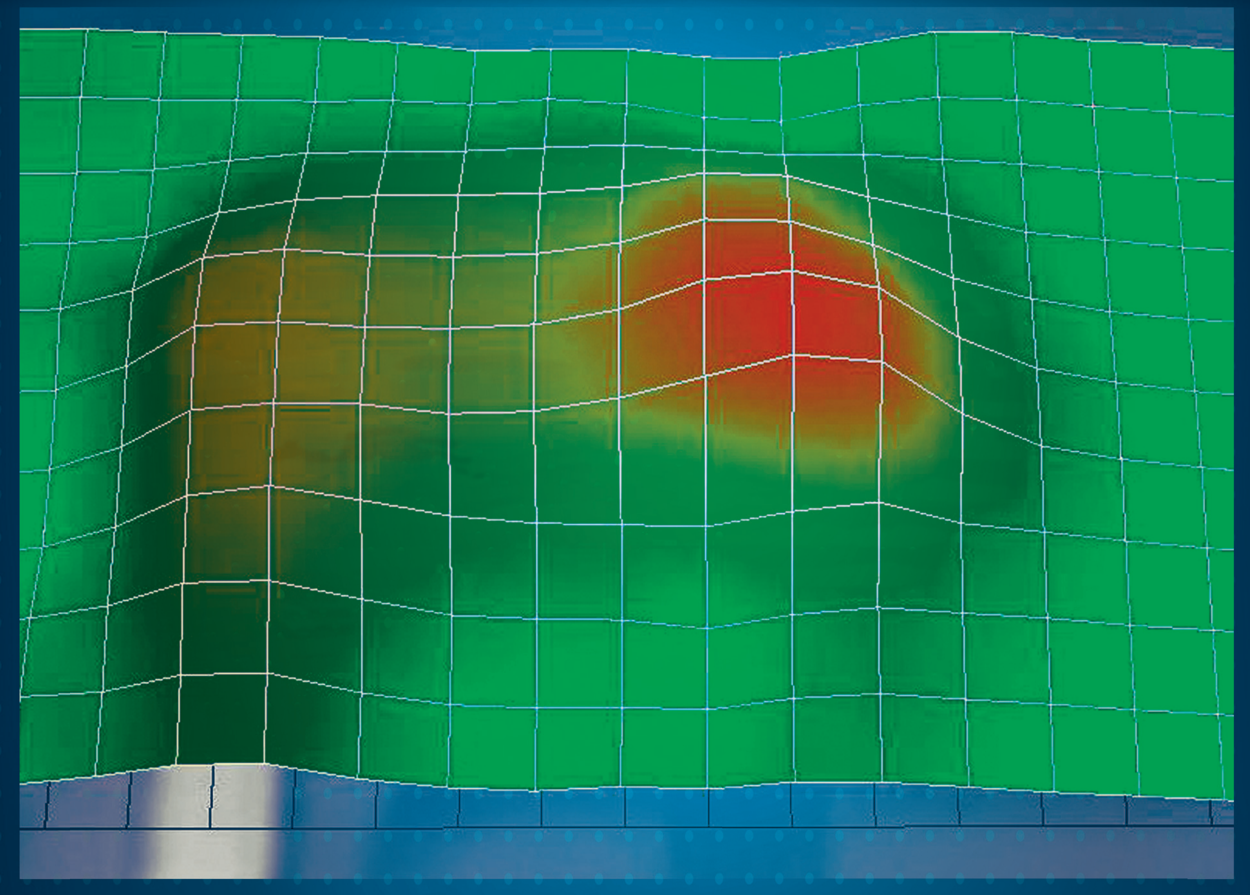
Characterization of strained silicon FinFETs and the integration of a piezoelectric layer



Buket Kaleli

CHARACTERIZATION OF STRAINED SILICON FINFETS AND THE INTEGRATION OF A PIEZOELECTRIC LAYER

Buket Kaleli

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CHARACTERIZATION OF STRAINED SILICON FINFETS AND THE INTEGRATION OF A PIEZOELECTRIC LAYER

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. H. Brinksma,
on account of the decision of the graduation committee,
to be publicly defended
on Wednesday the 20th of November 2013 at 16:45

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This dissertation is approved by:

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To my beloved husband, parents and brother

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1 Introduction

This chapter presents a general introduction to this thesis. The motivation, the project description and objectives are described. The reasoning behind the preferred device configuration and materials are discussed. Furthermore, concepts of steep sub-threshold devices reported from literature are summarized and the effects of strain in the Si channel are addressed. This chapter ends with an outline of the thesis.

1.1 The PiezoFET project

The official title of the project leading to this thesis is “Piezoelectric layer formation on a silicon channel”. It basically considers a piezoelectric layer on top of a fin shaped field-effect transistor (FinFET) channel. “PiezoFET” is the name referring to the fabricated device structure in this thesis. The described project is funded by the Dutch Technology Foundation (STW), with project number 10176. During the given period of time, the feasibility of this novel device structure with a piezoelectric stressor has been investigated. This work has been conducted at the MESA+ Institute for Nanotechnology, The Netherlands.

1.2 Concepts for steep sub-threshold slope FETs

The parameter that quantifies the electrostatic gate control over the sub-threshold drain current (I_d) of a FET is called the sub-threshold swing (*SS*). The *SS* is, by definition, the change in gate voltage resulting in one order of magnitude change in the drain current, *i.e.* the inverse of the sub-threshold slope. It is presented in Fig. 1.1 (no strain).

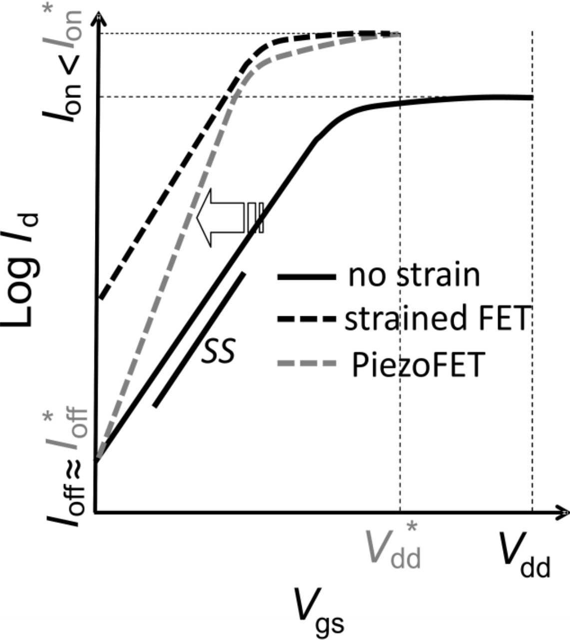

Fig. 1.1 Illustration of the I_d-V_{gs} characteristics of a MOSFET on semi-logarithmic scale. The characteristics are shown for a device with no strain (*i.e.* relaxed condition), constant strain and strain formed by the converse piezoelectric effect (*i.e.* the PiezoFET). The sub-threshold swing (*SS*) is also indicated.

For an ideal Si transistor, *i.e.* there is good electrostatic gate control over I_d, the *SS* equals 60mV/dec at room temperature. In practice this can be obtained for (long channel) fully depleted FinFETs and ultra-thin body SOI MOSFETs where the depletion capacitance is negligible, as will be discussed in chapter 4. Good gate control is important since it reduces the sub-threshold current which in turn determines the leakage power loss [1], an important contribution to the total power loss in a chip. Since, in advanced CMOS technology, there is a continuous trend in increasing functionality and speed of the electronic chip, the power consumption of the transistors should be reduced even more.

For CMOS, the so-called strain, *i.e.* mechanical deformation, is employed in silicon both by the academia and industry to increase the performance at a lower power. The conventional type of strain is typically constant depending on the surrounding materials and leads to a relatively high off-current (I_{off}) and on-current (I_{on}) provided all other process parameters have been kept the same [2-4], as illustrated in Fig. 1.1 (strained FET).

As discussed in chapter 2, the sub-threshold current is exponentially dependent on the band alignment, which is affected by strain formation and leads to an increased I_{off}. This strain-induced change in band alignment could also lead to increased charge carrier mobility values resulting in a higher I_{on}. Fig. 1.2 summarizes the effect of the stress components on the mobility in FinFETs (redrawn after [5]). It can be concluded from this figure that, since n-FinFETs are fabricated in this thesis, biaxial tensile stress along the channel length and fin width is favorable.

However, as illustrated in Fig. 1.1 a *SS* of less than 60 mV/dec, *i.e.* a sub-thermal sub-threshold swing, is desirable. Several device concepts have been proposed to obtain a sub-thermal *SS*. Tunnel FETs and impact ionization MOSFETs have been reported for this purpose [6-10]. However, there are some challenges like a low on- to off-current ratio I_{on}/I_{off} and hot carrier effects. In addition, negative capacitance FETs have been demonstrated to decrease the *SS* by replacing the standard insulator with a ferroelectric insulator [11, 12]. Therefore, before being successfully embedded in the CMOS technology, the gate stack materials and theory need to be studied further.

In this work, we propose and realize a new device concept which makes use of the converse piezoelectric effect to form a strain modulation in a silicon (Si) body. The basic idea behind this concept is that the strain in the Si body is increasing for a higher bias over the piezoelectric layer; that is placed on top of or around a Si body. This device concept is called the PiezoFET. The ideal I_d-V_{gs} characteristic is presented in Fig. 1.1 (PiezoFET).

In the PiezoFET, strain arises due to an upward and downward motion of the piezoelectric layer caused by an external bias. The strain is basically zero in the off-state, meaning that the leakage current does not change compared to a relaxed condition, while in the on-

state, by biasing the piezoelectric layer, a maximum amount of strain is obtained [13]. Consequently, the *SS* can be reduced by a piezoelectric stressor.

The resulting strain condition is not straightforward since it strongly depends on the (electro-) mechanical properties and layer thicknesses of the surrounding materials. The device geometry is equally important since it determines the (electro-) mechanical boundary conditions. These are different for a planar structure and a 3D structure like a FinFET. In Fig. 1.3 a schematic lay out of an SOI FinFET is presented, showing the Si fin, source and drain and gate configuration on a buried oxide (BOX) layer. Here the fin width, distance between fins and the aspect ratio are important. It is expected that for a high aspect ratio and relatively small fin (and pitch) dimensions strain can be obtained in a FinFET-based PiezoFET. In this case, a piezoelectric layer and electrodes are introduced in the structure to control strain. More analysis on the strain induced by the piezoelectric layer is discussed in chapter 5.

By considering all the strain related effects that have been mentioned until now, the change in the mobility and I_d-V_{gs} characteristics can be estimated. The ultimate goal of the piezoelectric effect induced strain on the I_d-V_{gs} characteristics is illustrated in Fig. 1.1 (PiezoFET).

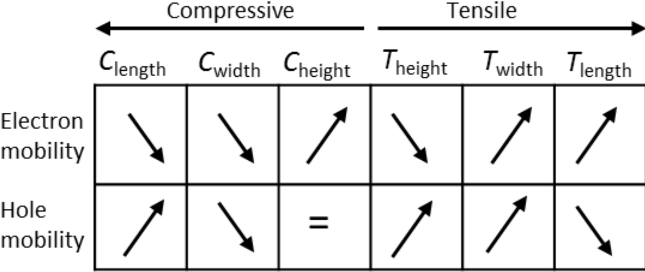

Fig. 1.2 The effect of stress components on the $(110)/[1\bar{1}0]$ FinFET electron and hole mobility. Redrawn after [5].

In summary, it is expected that the PiezoFET can offer a great potential as a low-power switch. In this study, the PiezoFET in a fin-shaped field-effect transistor (FinFET) configuration has been realized and analyzed.

1.3 Choice of a device configuration and materials

1.3.1 FinFETs as a replacement of MOSFETs

Planar bulk transistors have been serving the needs for integrated circuits for several decades. Over the years, the size of the transistors has been decreasing following

Moore's law [14]. The motivation is saving space and reducing the unit cost. An increase in switching speed (due to shrinking the size of the gate) is a useful by-product of the miniaturization. However, continuous downscaling of these devices leads to an increase in short channel effects (SCE). SCE dominates when channel lengths are comparable to depth of source and drain junctions and depletion widths. It causes a degradation of the sub-threshold characteristics and results in higher standby power consumption [15]. After the introduction by Hisamoto *et al*. [16], the fin-shaped field-effect transistor (FinFET) has attracted much interest to solve this issue. A schematic view of the FinFET with a single fin on a silicon-on-insulator (SOI) substrate is shown in Fig. 1.3.

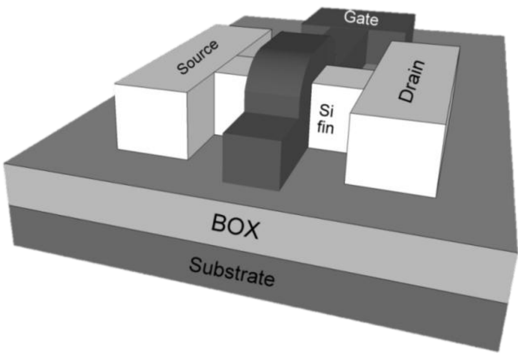

Fig. 1.3. Schematic layout of an SOI FinFET, bird's eye view.

The FinFET is a potential replacement of the bulk MOSFET. It comprises a gate around silicon (Si) body and depending on its design, it is considered as a double-gate or a triple-gate (this figure) device. With the help of the double-gate or triple-gate architecture, the FinFET enables a better electrostatic gate control over the channel, which comes with relatively low power consumption in standby mode [17, 18]. FinFETs are already a part of the most modern processors.

Furthermore, if the fin body was designed ultra-narrow, it would be entirely depleted enabling volume inversion [19]. The same architecture can also be obtained with a planar SOI FET having an ultra-thin silicon body. A fully depleted body with low doping helps *i*) to obtain an inverse sub-threshold slope (*i.e.* subthreshold swing, *SS*) close to the theoretical value of 60 mV/dec at T=300 K (this will be discussed in section 1.3), *ii*) to tailor the threshold voltage (V_{th}) by adjusting the work function of the gate material only, *iii*) to reduce the impurity scattering thereby increasing the mobility and iv) to eliminate random dopant fluctuations [20-22]. In addition, since the charge carriers are confined in the body, the effects related to surface imperfections, such as traps, and scattering are less important for ultra-narrow fins. This means that the switching speed and mobility can be increased [23]. However, when the fin width is too small, due to the quantum confinement effect, carrier scattering inside the channel becomes more important than

surface scattering; resulting in a reduced mobility. Therefore, optimum conditions need to be found regarding the device architecture.

Along with its superior properties, the development of the FinFET leads to design and process related requirements like *i*) the threshold voltage adjustment, which requires gate work function tuning around the whole fin, *ii*) fringing capacitance between gate and top/bottom of the source/drain (S/D) regions, which requires minimizing fin pitch and using merged S/D, *iii*) parasitic S/D series resistance, which requires epitaxially raised S/D and silicide engineering and *iv*) performance variability, which requires uniform fin width and gate work function [24-28]. Therefore, the design parameters need to be considered to eliminate or to minimize these effects.

In this work, along with all the advantages mentioned above, the choice of the FinFET-like structure for the PiezoFET with narrow fins is a good candidate to obtain the optimum amount of strain in the Si channel.

FinFETs can be fabricated on SOI or bulk substrates. Up to date, there have been several reports mentioning the advantages of SOI FinFETs over their bulk counterparts [29-31]. Although they are more expensive, SOI substrates and lowly doped fins result in less junction capacitance, high mobility and reduced mismatch [32]. Although self-heating effect is a known problem for SOI devices [33], it will not be an issue for low power device concepts.

In this research, SOI substrates were used to realize FinFETs. The SOI substrates were obtained from NXP Semiconductors, Nijmegen. They were first laser cut from 125 mm to 100 mm to make them compatible with the available systems in the MESA+ Nanolab. More details about the processing and analysis of the fabricated devices are given in chapter 4.

1.3.2 Encapsulated TiN as a gate material

In low power CMOS, a symmetrical and low threshold voltage metal gate is desired for n-channel and p-channel devices [34, 35]. For many years poly-Si has been used as a gate material. The main reason for this is that a heavily doped poly-Si gate can be tailored such that it has work function close to the band edges (*i.e.* ≈4.2 eV for n-type and ≈5.2 eV for p-type). Its work function can be further modulated by adjusting the doping conditions. This makes it suitable for both n- and p-type devices. Another advantage of the poly-Si gate is the higher temperature budget. However, as a downside, the poly-depletion effect (i.e. creation of depletion layer in the gate, which adds in series to the oxide capacitance) might increase the effective oxide thickness, thereby decreasing the series capacitance and the drive current. In addition, the p+ poly Si gate is not compatible with high-κ

dielectrics due to Fermi level pinning [36]. Furthermore, the gate sheet resistance of even a heavily doped poly-Si is higher than that of a metal gate. The formation of silicide is used to increase the conductivity to solve this issue. For reducing the gate leakage and not to suffer from partial depletion effects, high-κ materials are co-integrated with the gate technology in semiconductor industry.

The use of a metal gate eliminates these poly depletion and conductivity problems. However, in general, most metals are not compatible with high temperature processing (> 600 ^0C). Metal nitrides (in our case TiN), on the other hand, are more suitable for higher temperatures. TiN is encapsulated with a poly-Si layer for planarization purposes and to prevent oxidation. The poly-Si layer also serves as a hard mask for ion implantation. The work function of metal nitrides typically is between 4.4 eV and 4.7 eV. This work function is not suitable for low power planar MOSFETs (it needs to be close to the Si band edge for planar structures) but they can be utilized for low power, multigate CMOS applications [37]. Therefore, in this study, we choose the poly-Si/TiN stack as a gate material for the fabricated SOI FinFET devices, using thermal SiO_2 as the gate dielectric.

1.3.3 Converse piezoelectric effect as a stressor

When an electric field is applied to a piezoelectric material, the structure of the piezoelectric material is deformed mechanically by the converse piezoelectric effect [38]. This deformation will be transferred to the surrounding material. The electrical signal is then transformed into a mechanical or acoustic signal. The use of the converse piezoelectric effect has been reported before for different device structures.

In a bulk acoustic wave or a surface acoustic wave resonator, for instance, the converse piezoelectric effect is used to obtain a resonance [38, 39]. A report from Shayegan *et al*. [40] demonstrated the use of piezoelectric material to apply a uniaxial stress in a plane of a confined 2D electron system formed by an AlAs quantum well. In this way, the electronic properties of the 2D electron system can be modified.

Note that, the piezoelectric effect is widely used in III-V heterojunction device structures. In these devices, lattice mismatch induced strain causes piezoelectric polarization, which results in an increased electron concentration in a 2-dimentional electron gas (2DEG) and a threshold voltage shift [41, 42]. However, to the best of our knowledge there has not been any experimental evidence on the electrical characteristics in these III-V devices caused by the opposite effect, hence the converse piezoelectric effect.

In this study, the converse piezoelectric effect is used for stressing Si FinFET channels [13]. The main objective is to change the transport properties to obtain high mobility and steep

sub-threshold slope devices. Analyses about the strain effect in Si channels are given in chapter 2.

1.4 Technological requirements and research questions

As mentioned before, the objective of this thesis is to realize strained FinFETs with a piezoelectric stressor. There are quite some technological problems:

i) Fabricating the near-ideal FinFET device structures comprising narrow fin widths with a high aspect ratio to obtain a high amount of strain. This also implies that a combined effort of e-beam lithography and photolithography is required in the MESA+ cleanroom, which is not straightforward,
ii) Growing or depositing high quality, uniform piezoelectric material on top of the FinFET structures,
iii) Optimizing the thickness of the layers between the piezoelectric stressor and the Si channel to a minimum to prevent stress relaxation while maintaining the quality of these layers,
iv) Integration of the piezoelectric layer without degrading the Si channel.

As a result, many research questions arise:

i) What is the step coverage of the piezoelectric layer around the fin? What is its grain/domain orientation?
ii) Do we maintain good ferroelectric or piezoelectric properties for aggressively scaled dimensions for both the buffer and the piezoelectric layers?
iii) Can we integrate the piezoelectric layers with Si? This is especially difficult for good piezoelectric materials such as Lead zirconate titanate (PZT). Is there diffusion of contaminants from the PZT layer into the Si body? And, if so, do they affect the device behavior?
iv) What is the effect of the piezoelectric layers on the electrical characteristics of the FinFET? For instance, does it influence the *SS* or mobility as expected? Does it depend on the device dimensions and geometry?
v) Is the converse piezoelectric effect feasible for significantly stressing the channel?

These subjects are addressed and most of the questions will be answered in the following chapters of this thesis.

1.5 Organization of the thesis

This thesis is organized as follows:

Chapter 2 introduces the use of strain in Si based devices. Strain formation and its effects on the transport properties such as band gap and mobility are discussed. More specifically, FinFETs with a constant strain are presented. Analysis of the strain in these devices has been performed with the help of electrical and optical characterization techniques. The results provide a clear evidence of the effect of strain on the band alignment of Si.

Chapter 3 introduces an experimental study on the sub-100 nm ferroelectric thin film PZT capacitors. The influence of the film thickness and the encapsulated TiN bottom electrode on the ferroelectric and piezoelectric properties of PZT has been investigated. Some important figures-of-merit have been obtained with the help of electrical and optical characterization techniques. These figures have been utilized to optimize the PiezoFET design in this thesis.

Chapter 4 presents the realization and characterization of FinFETs. FinFETs with different fin widths and channel lengths have been realized to obtain a variable strain configuration after the piezoelectric layer deposition. The presented devices show good electrical characteristics and they provide a basis for the novel device structure called the PiezoFET, in chapter 5.

Chapter 5 describes the novel PiezoFET. It starts with a brief analysis of the piezoelectric layer as a stressor. Details of the device fabrication and characterization are presented. The observed effects in the transport properties of the PiezoFET have been investigated and are discussed. Finally, conclusions are given based on the analysis of the experimental results.

Finally, chapter 6 summarizes this study and presents recommendations for future research.

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2 Strained silicon devices

In this chapter, a brief introduction to strained silicon devices is given. The effect of strain on the band gap and mobility is discussed. The electrical and optical characterization of TiN induced strain on FinFETs is presented. It is demonstrated that the conduction band offset is changing depending on the fin dimensions, which can be explained by counteracting quantum confinement and strain effects.

2.1 Strain formation in silicon-based devices

To improve the transport properties of a (crystalline) semiconductor material, and hence the device performance, so-called strain is often applied in the semiconductor technology and in research projects. Strain is defined as the deformation of a material normalized to its stress free dimension [1]. Strain causes elastic stress (or forces). The strain (ε) and stress (σ) are related according to the scalar notation $\sigma = E\varepsilon$, where E is the stiffness or Young's modulus of the material. Basically, one can imagine the strain effect to be pushing atoms in the periodic crystal together (*i.e.* compressive or negative strain) or pulling them apart (*i.e.* tensile or positive strain). This can occur in one direction (uniaxial) only or in several directions (biaxial or triaxial).

There are different ways to form strain in silicon (Si). Some examples are phonon induced lattice vibrations, lattice mismatch during film growth, intrinsic strain in deposited thin films and externally applied strain.

The calculations of Bardeen and Shockley on deformation potentials and the measurements of Smith on the piezoresistance effect are the first physical reports explaining the enhancement of mobility due to strain [2, 3]. Since then, there have been many experimental and theoretical reports on the effect of strain on the band gap and charge carrier mobility [4-11]. Although there was a strong interest in using strained silicon-germanium (SiGe) alloys for high mobility channels, it could not have been realized in Si-based MOSFETs until 1991 due to the high density of interface states generated during oxidation. Iyer *et al.* [12] were the first who demonstrated a promising high-quality dielectric system by capping the SiGe with a thin Si layer followed by oxide deposition. Later on, Welser *et al*. [4] first demonstrated an improvement in device performance by strain in n-channel MOSFETs. Here, a strained-Si channel was grown on a relaxed silicon-germanium ($Si_{0.71}Ge_{0.29}$) layer. Because of the lattice mismatch between the relatively thick SiGe layer and thin Si layer, global biaxial tensile strain has been formed in the latter. In the following years, strained Si/relaxed $Si_{1-x}Ge_x$ systems have been studied extensively and have become a promising candidate for a performance boost in CMOS, mainly by enhancing the mobility [13-16] and consequently the on-current. In addition, some groups reported on the use of $Si_{1-x}Ge_x$ systems in the source and drain regions acting as a local stressor in the channel region for improving the hole mobility in p-channel MOSFETs [17, 18]. This concept is presently in production, for example, in Intel's 45nm Xeon technology.

Along with $Si_{1-x}Ge_x$, silicon nitride (SiN_x), titanium-nitride (TiN) and piezoelectric materials are also well-known examples for stressors utilized for different purposes. SiN_x has been studied as an external and local stressor in many studies mainly as a capping layer in

planar and 3D device structures [18-21]. The strain formed by TiN and piezoelectric layers in FinFETs will be discussed in sections 2.3 and 5.1, respectively.

2.2 The effect of strain on the band gap and mobility

Strain is known to change the mobility and modify the band gap of the material depending on the strain type, direction and the material's properties. It is important to note that both the conduction and valence band in Si are degenerate: the first comprises six so-called Δ valleys while the latter can be subdivided into a heavy hole (HH) and a light hole (LH) band. When stress is applied, the degeneracy basically becomes less. The changes in conduction and valence band in bulk Si for biaxial tensile strain is shown in Fig. 2.1. Valence band in Fig 2.1 (b) is plotted in energy vs. reciprocal space (or k-space, with k=2π/lattice constant).

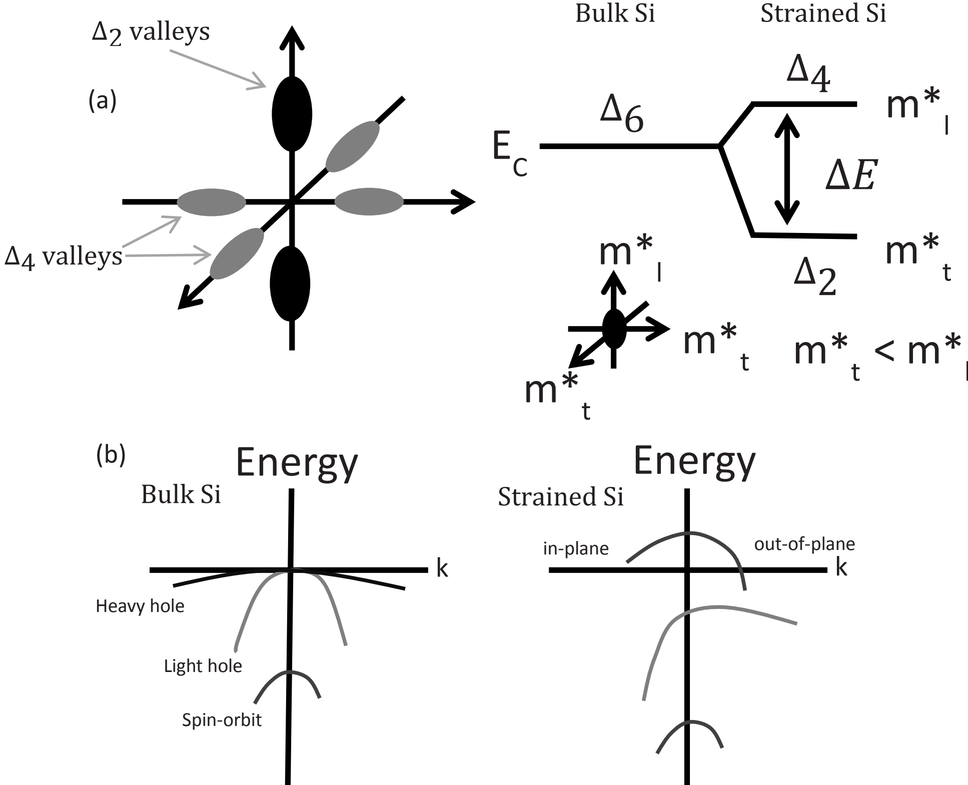


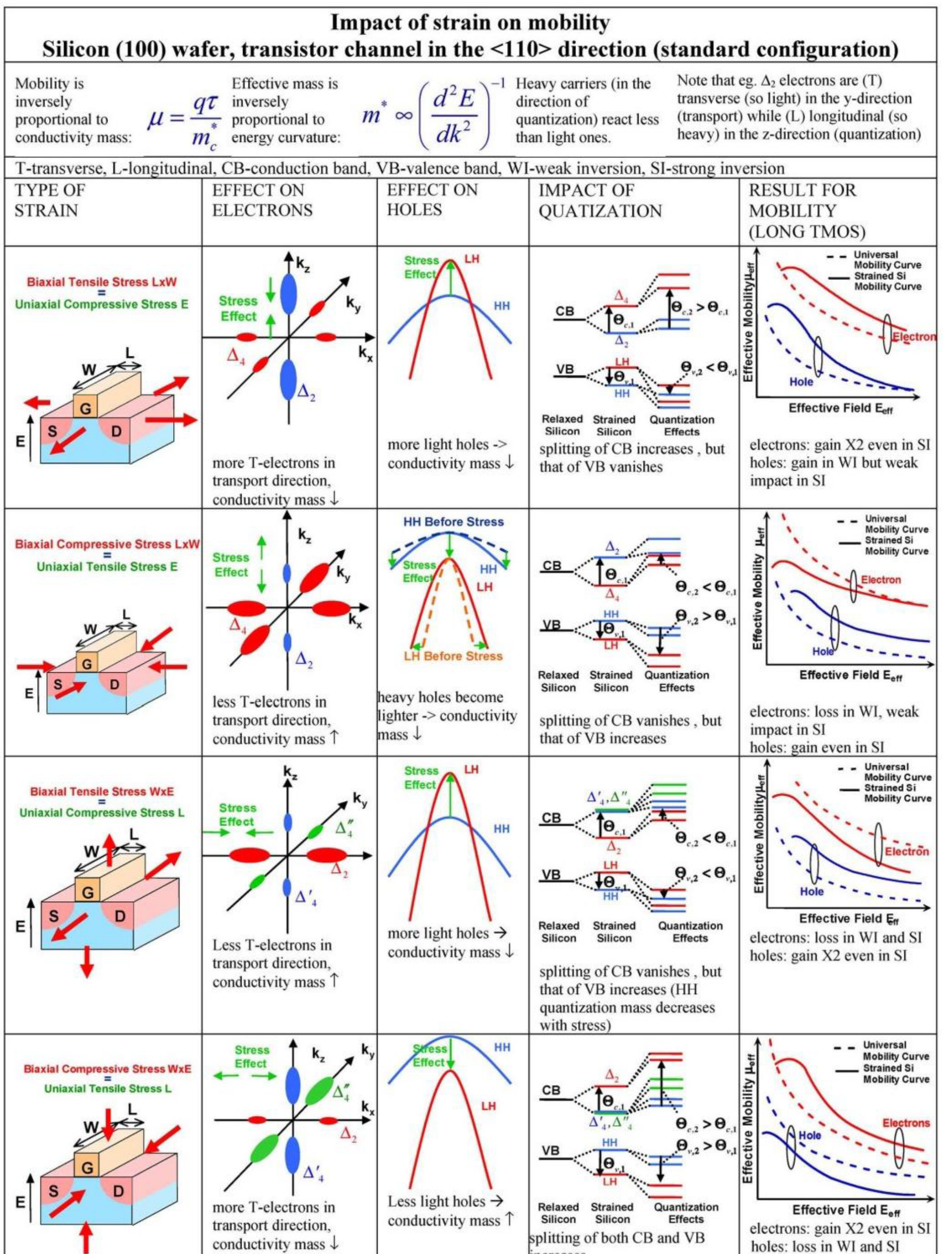
Fig. 2.1 Biaxial tensile strain induced changes in the (a) conduction band and (b) valence band of planar/bulk Si. Redrawn after Rim *et al*. [22].

The Si conduction band valleys split into Δ_2 and Δ_4 valleys depending on the amount and orientation (in this case [001] oriented) of stress or strain. On the other hand, the valence

HH band shows a linear while the LH band shows a nonlinear dependency with strain. In case of a large amount of strain, the electrons completely populate the lower Δ_2 valley [7]. Since the in-plane conductivity effective mass of the Δ_2 valleys is smaller than that of the Δ_4 valleys and intervalley scattering is suppressed due to this splitting, the electron mobility increases [23]. Similarly, strain lifts the degeneracy between HH and LH bands and the spin orbit band is lowered in energy resulting less intervalley scattering and improvement in-plane hole mobility. In fact, as indicated in Fig. 2.1 (a) and (b), the conduction band edge drops and valence band edge increases resulting in a reduced band gap.

Skotnicki *et al*. [6] reported the effect of strain on the band gap and mobility of a bulk MOSFET with a <110> oriented channel. Table 2.1 shows a part of this report. The table indicates that the band gap decreases for all stress conditions. However, the net change depends on the presence of quantization effects. The change in mobility, on the other hand, depends on the stress condition. It is observed that tensile stress along the channel length is needed to obtain higher electron mobility. In contrast, it leads to a decrease in hole mobility.

Table 2.1 Analysis of strain configuration and its effects in CMOS (Skotnicki *et al*. [6], with courtesy).



Impact of strain on mobility
Silicon (100) wafer, transistor channel in the <110> direction (standard configuration)

Mobility is inversely proportional to conductivity mass: $\mu = \frac{q\tau}{m_c^*}$	Effective mass is inversely proportional to energy curvature: $m^* \propto \left(\frac{d^2E}{dk^2}\right)^{-1}$	Heavy carriers (in the direction of quantization) react less than light ones.	Note that eg. Δ_2 electrons are (T) transverse (so light) in the y-direction (transport) while (L) longitudinal (so heavy) in the z-direction (quantization)

T-transverse, L-longitudinal, CB-conduction band, VB-valence band, WI-weak inversion, SI-strong inversion

TYPE OF STRAIN	EFFECT ON ELECTRONS	EFFECT ON HOLES	IMPACT OF QUATIZATION	RESULT FOR MOBILITY (LONG TMOS)
Biaxial Tensile Stress LxW = Uniaxial Compressive Stress E	more T-electrons in transport direction, conductivity mass ↓	more light holes -> conductivity mass ↓	splitting of CB increases , but that of VB vanishes	electrons: gain X2 even in SI holes: gain in WI but weak impact in SI
Biaxial Compressive Stress LxW = Uniaxial Tensile Stress E	less T-electrons in transport direction, conductivity mass ↑	heavy holes become lighter -> conductivity mass ↓	splitting of CB vanishes , but that of VB increases	electrons: loss in WI, weak impact in SI holes: gain even in SI
Biaxial Tensile Stress WxE = Uniaxial Compressive Stress L	Less T-electrons in transport direction, conductivity mass ↑	more light holes → conductivity mass ↓	splitting of CB vanishes , but that of VB increases (HH quantization mass decreases with stress)	electrons: loss in WI and SI holes: gain X2 even in SI
Biaxial Compressive Stress WxE = Uniaxial Tensile Stress L	more T-electrons in transport direction, conductivity mass ↓	Less light holes → conductivity mass ↑	splitting of both CB and VB increases	electrons: gain X2 even in SI holes: loss in WI and SI

K. A. Rim *et al*. [24] experimentally showed for the first time that the sub-threshold current of an n-type Si MOSFET increases, or the threshold voltage drops (by ≈ 200mV), when biaxial tensile strain is applied. This is due to this smaller bandgap and lower conduction band in strained Si compared to the relaxed or bulk Si counterpart. In

addition, calculations indicate that both biaxial and uniaxial tensile stress causes a band gap decrease for Si, Ge and GaAs [11]. However, for compressive stress, the band gap changes depending on the stress configuration.

The effect of strain on the mobility of n-MOSFET and p-MOSFET device structures under different stressing conditions has been studied extensively. Depending on the orientation, strain type and level, mobility enhancement was demonstrated in many reports. This helped to understand and to control the effects [5,25,26].

Furthermore, the effects of strain on a material with a thickness of only several atomic layers differ from bulk material. Quantization effects have to be taken into account when dimensions are downscaling. In that case, the band structure and mobility will be affected depending on both the applied strain and quantization. With quantization, the apparent or effective band gap of the material increases [27-29]. This effect is also demonstrated and explained in section 2.3.1.1 for n-type FinFETs. Strain in these devices resulted in an enhancement in mobility and on-current as reported by Rim *et al.* [30] and Feste *et al.* [31]. They demonstrated a 110 % and 230 % improvement in electron mobility in a 7 nm thick planar strained Si layer and 42 nm thick, ≈ 35 nm wide strained Si fin, respectively. This resulted in a proportional increase in on-current of the strained FinFET. These figures show that strained FinFET structures are important for CMOS applications.

2.3 TiN induced strain on FinFETs

In section 2.1, several techniques of strain formation have been discussed. This section focusses on the external and local strain formation in FinFETs due to the use of a stiff conductor such as TiN [32-35]. The motivation of using the FinFET configuration was discussed in chapter 1, section 1.3.1.

TiN induced strain in Si originates from its growth mechanism and the difference in coefficient of thermal expansion (CTE) between the TiN gate and the Si. This type of strain has been studied before [26, 36, 37] focusing on the mobility. In this work, FinFETs manufactured by NXP-TSMC Research Leuven, Belgium [38], have been studied focusing on the band alignment. The silicon-on-insulator (SOI) FinFETs have a (001) surface and $(1\bar{1}0)$ fin sidewall orientation. It is basically the same device set as reported by Serra *et al*. [37] which has been analyzed further. Fig. 2.2 shows a TEM cross section of a FinFET on an SOI substrate. The gate stack consists of a gate dielectric layer with a 1 nm thick silicon-dioxide (SiO_2) and 1.7 nm thick hafnium-silicate (HfSiO) layer and a 5 nm thick TiN layer (deposited by physical vapor deposition) as the gate material with a poly-Si capping. All the devices characterized in this work comprised five fins with various fin widths (5 nm ≤ W_{FIN} ≤ 1000 nm) and gate lengths (35 nm≤ L_{gate}≤ 10 µm). The fin height or SOI thickness was 60nm (H_{FIN}). For more processing details, refer to [38].

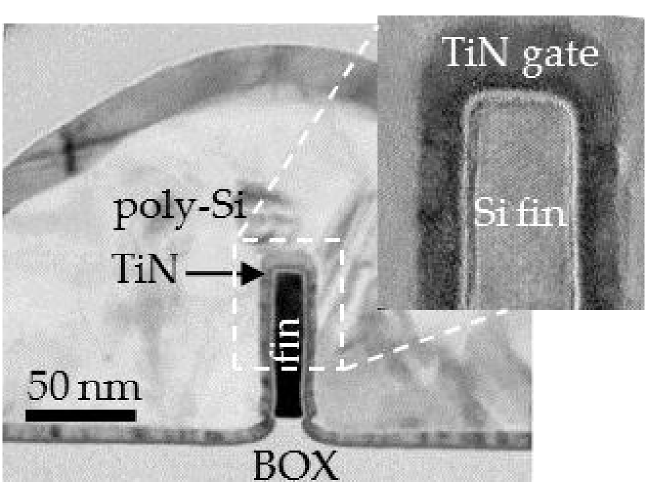


Fig. 2.2 TEM cross section picture of the FinFET (with courtesy of M. van Dal).

An important detail is the thermal cycle implemented after gate deposition. This results in a permanent strain in the channel [37]. This strain can be illustrated by simulations performed using a multiphysics Finite-element-method (FEM) tool (Comsol MultiPhysics 3.5a). In the simulations, the Si substrate was neglected to decrease the computational load. Fixed boundary conditions were applied below the buried oxide (BOX) layer to mimic the stiff Si substrate. For the Young's modulus and CTE of Si and TiN are taken 130 GPa & 2.5×10^{-6} K^{-1} and 600 GPa & 9.4×10^{-6} K^{-1}, respectively. The experimental 5-fin device structure was simplified to a single fin device. Symmetric boundary conditions were applied to the sides of the fins as well as at the source and drain regions. The rest of the boundaries were kept free to move. A high temperature cycle from 25 °C to 1100 °C and back to 25 °C has been implemented on the device structure to form strain as in the real case. During the thermal cycle of the stacked structure, the strain increases while the temperature increases. At elevated temperatures (above 1100 °C) plastic relaxation occurs and the strain will be low. The simulations are referenced to this relaxed state. When the system is cooling down, the strain increases again and remains permanently in the Si body or fin. Figs. 2.3 (a)-(c) show the simulated vertical strain (ε_{zz}) in the fin cross section of a 5 nm wide fin at 900 °C, 500 °C and 25 °C, respectively. Compressive strain (ε_{zz}) in the range of -0.9 % has been observed for a 5 nm fin width (W_{FIN}). The other strain components, ε_{xx} and ε_{yy} are much smaller than ε_{zz} (up to -0.18 %) and therefore neglected. The simulation for the 30 nm wide fin at 25 °C is also depicted (Fig. 2.3 (d)) to show that the generated strain decreases when W_{FIN} increases. It also becomes less uniform in the silicon body. FEM simulated maximum strain values are plotted against W_{FIN} in Fig. 2.10[1].

[1] The simulations were performed by Tom van Hemert, with courtesy.

As demonstrated before by Serra *et al*. [37] compressive strain in the fin height direction favors an increase in electron mobility.

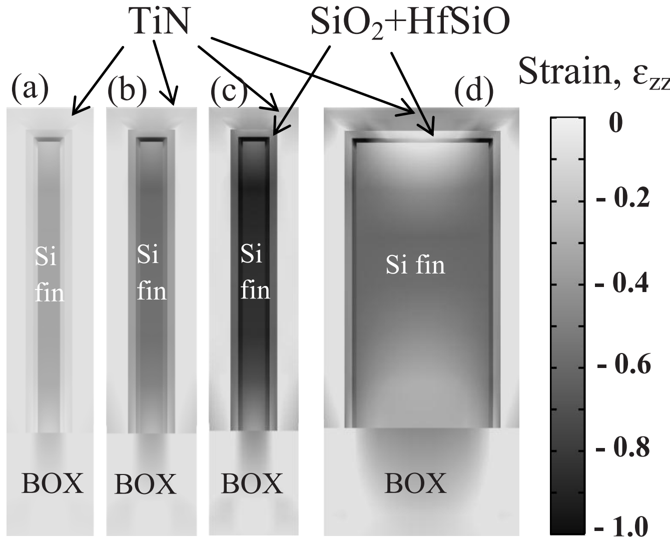


Fig. 2.3 ε_{zz} strain values of the 30 nm and 5 nm wide FinFETs obtained with multiphysics FEM simulations during cooling down cycle from T=1100 °C to 25 °C for W_{FIN}=5 nm at (a) 900 °C, (b) 500 °C , (c) 25 °C, and (d) 25 °C for W_{FIN}=30 nm. The vertical bar indicates the strain values varying from 0 to -1.0 (compressive) strain. The thickness of the TiN film is 5 nm and the height of Si fin is 60 nm. Note the relatively high strain value in the HfSiO gate dielectric.

2.3.1 Characterization of strain by optical and its effects by electrical techniques

Strain characterization plays an important role in understanding and controlling strain effects. There are different methods possible for this purpose. Raman spectroscopy [39, 40] is mainly used for strain characterization. However, holographic interferometry [37], synchrotron x-ray scattering [41] and nano-beam diffraction [42] techniques have also been used by several research groups. Each of these techniques has advantages and disadvantages regarding the resolution and sensitivity.

In addition to these direct measurement techniques, electrical characterization can also be employed to study the effect of strain in devices. In this case, strain effects are expected to appear as a change in the band gap and mobility as described in section 2.2. Using both optical and electrical characterization and in depth knowledge of strain and its effect can be obtained. In the following two sub-sections, *I-V* curves will be studied to analyze the effect of strain on FinFETs and Raman spectroscopy will be used to characterize the strain.

2.3.1.1 Temperature dependent *I-V* measurements on strained devices

Temperature dependent *I-V* measurements were performed using n-type strained FinFET devices with different fin widths (W_{FIN}) and gate lengths (L_{gate}) [32, 34]. By using the subthreshold current technique described by van der Steen *et al*. [43] energy band offsets of the FinFETs can be extracted. Since the band offsets depend on the amount of strain, this method can be utilized. As discussed before on our FEM simulations, the amount of strain in the FinFETs under study are expected to increase for a smaller W_{FIN}.

Valence or conduction band offsets can be calculated using the subthreshold current of the reference device having a wide fin (hence negligible strain), namely I_{ref}, and that of a device with a smaller fin width, I_{thin}. The ratio of subthreshold currents is then given by:

$$\eta \equiv \frac{I_{ref}}{I_{thin}} = \frac{\mu_{ref} .g(W_{FIN,ref})}{\mu_{thin} .g(W_{FIN,thin})} \exp(\frac{\Delta E_x}{kT}) \qquad (2.1)$$

where $g(W_{FIN})$ represents the effective density of states (DOS) depending on the fin width, μ is the charge carrier mobility, and ΔE_X is the difference in conduction or valence band edge of the reference and narrow fin device. Since n-type FinFETs have been studied for this purpose, only the conduction band offset has been determined. In order to determine the valence band offset p-type FinFETs are required. The temperature dependence of η depends strongly on the conduction band offset because of the exponential term. Assuming equal temperature dependence of μ and DOS for both devices, $\Delta E_x /k$ is found to be equal to the slope of the $\ln(\eta)$ vs. $1/T$. It is important to note that the strain changes with temperature. However, this change is small (0.1 %) compared to the overall strain (-0.6 %) [34].

I-V measurements of $(1\bar{1}0)/[110]$ oriented n-FinFET devices were done at temperatures ranging from 25 °C to 150 °C. Since short channel effects can result in misinterpretation of the results, the conduction band offset was calculated from long channel devices (i.e. 1 µm and 10 µm). The maximum W_{FIN} here was 30 nm, which was used as a reference, and the minimum W_{FIN} was 5 nm. In Fig. 2.4 $\ln(\eta)$ vs. $1/T$ curves have been plotted for the FinFETs with 1 µm and 10 µm gate length.

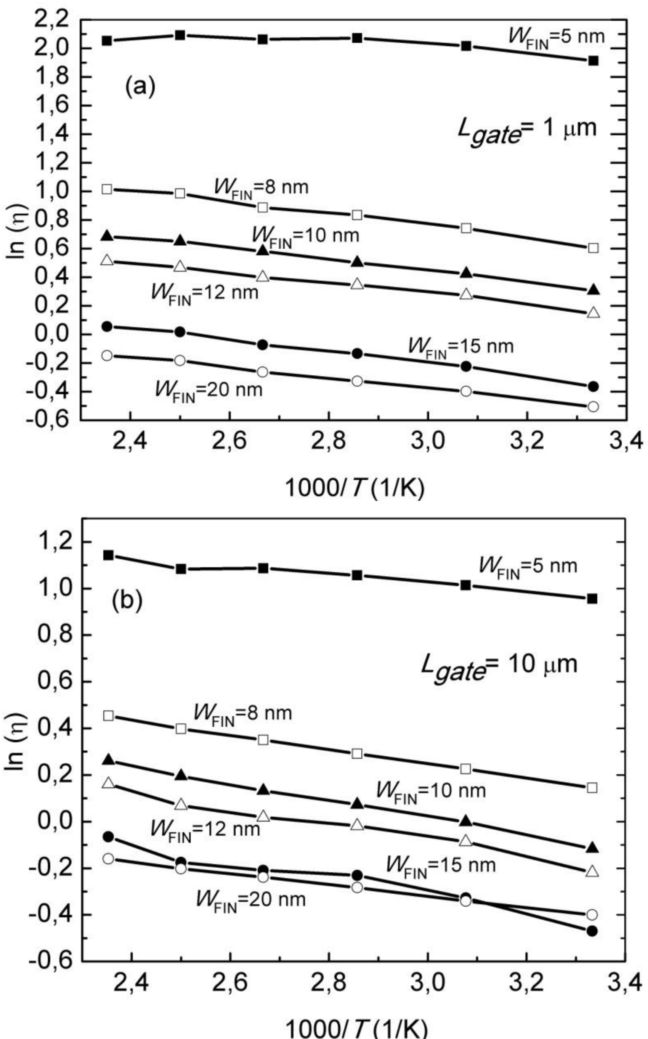


Fig. 2.4 $\ln(\eta)$ vs. 1/T curves of (a) 1 μm and (b) 10 μm long devices.

In Fig. 2.4 the $\ln(\eta)$ value increases for narrow fins. This effect is due to a decrease in mobility for very narrow fins [44]. However, this increase is stronger for a 1 μm device than that of a 10 μm long device. A reason could be a more profound non-uniformity in channel width and parasitic charges, since at low vertical fields Coulomb scattering is important.

From the slope of the curves depicted in Fig. 2.4, the calculated conduction band offset has been plotted against W_{FIN} as shown in Fig. 2.5. Values down to ≈ -40 meV are obtained. The error bars in Fig. 2.5 were determined from the error associated with linear fitting of $\ln(\eta)$ vs. $1/T$ curves. In this figure, a maximum value for the (absolute) band offset has been obtained for a W_{FIN} of around 12 nm. This can be explained by two

counteracting mechanisms [32, 34]. As discussed earlier, when W_{FIN} is decreasing, the built-in strain due to the TiN layer increases. For all strain conditions this shifts the lowest occupied conduction band, hence the Δ_2 valleys, downwards with respect to un-strained condition [37]. However, for W_{FIN} < 12 nm, quantization of the carriers occurs and this results in an upward shift of the conduction band edge (despite the higher amount of strain). The same trend was obtained by van Hemert *et al.* [34] in their band offset calculations in which strain and quantization effects were taken into account. Note that the impact of these effects depends on the channel orientation [34], in our case the channel is oriented along [110] direction.

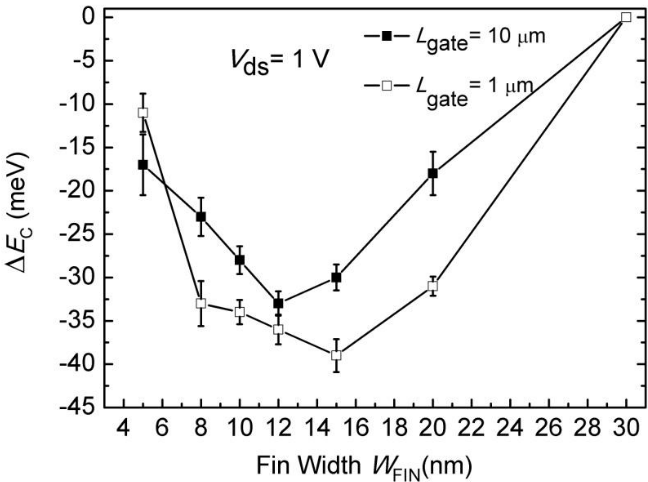


Fig. 2.5 Extracted conduction band offset for a device with a 1 µm and 10 µm gate length.

2.3.1.2 Raman spectroscopy characterization of strain

A more direct physical characterization technique would complete the strain analysis and could be helpful to support the observations in the electrical data obtained from the NXP-TSMC FinFETs. Raman spectroscopy is a non-contact and non-destructive technique that is most widely employed for this purpose [35, 39, 45-48], yielding valuable information about strain even in aggressively scaled device configurations [40, 49].

The technique relies on the inelastic scattering, or Raman scattering, of monochromatic light (usually from a laser). The scattering process involves an instantaneous absorption of a photon and subsequent emission of scattered photon. When the emitted photon is elastically scattered, the incident and scattered photon has the same frequency. However, if an inelastic scattering occurs, the frequency of the scattered photon shifts. During inelastic scattering, incident photons excite atom or molecule from the ground to a virtual energy level. While relaxing, it emits a photon and returns to a different rotational or vibrational state. Depending on the energy of the final state with respect to

initial state, the emitted photons of the laser light will be shifted to higher or lower frequency. This shift provides information about the vibrational, rotational and other transitions. However, inelastic scattering (or Raman scattering) results in a weak signal while the intense part of the signal is due to elastic scattering (or Rayleigh scattering). Therefore, the Rayleigh scattered photons are filtered out to separate the weak Raman scattered photons. Fig. 2.6 illustrates the transitions corresponding to Rayleigh scattering, stokes and anti-Stokes Raman scattering.

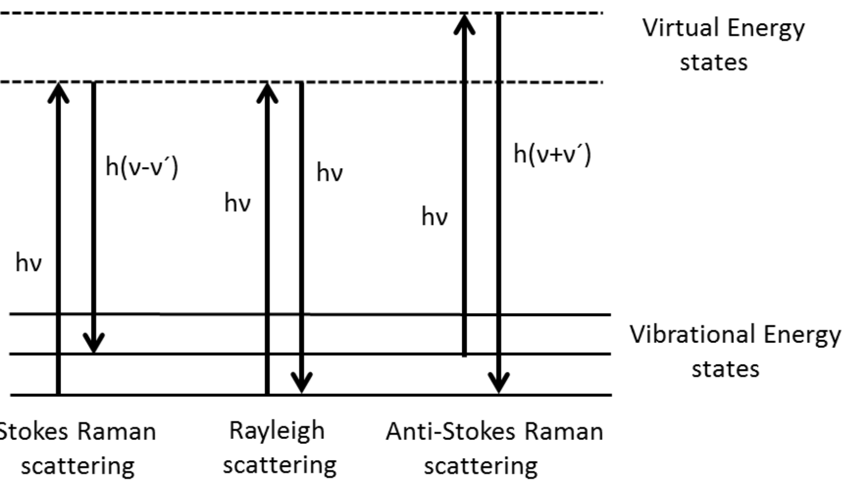


Fig. 2.6 A diagram illustrating the transitions corresponding to Rayleigh scattering, Stokes and anti-Stokes Raman scattering.

When the crystal lattice is mechanically strained, the atomic distances change. Since the lattice vibration frequency depends on the atomic distance, a vibrational frequency shift occurs. This shift directly affects the Raman peak position. Strain level in the lattice can be determined by using the calibrated Raman peak shift-strain relation.

The Raman spectroscopy measurements have been carried out at room temperature using a confocal Raman microscope (alpha300R, Witech GmbH) with 0.8 cm^{-1} wavenumber resolution (which corresponds to about 0.15 % strain resolution) and a 532 nm laser source with an output power of 47 mW. This wavelength will give a penetration depth of light in the silicon in the range of 800-1000 nm. This high penetration depth leads to a weak Raman signal from the FinFET with respect to the strong signal from the surrounding relaxed silicon. It is important to note that, since a high penetration depth might be an issue, we performed Raman measurements on the same samples at a shorter wavelength (454 nm) using the Renishaw Raman tool[2]. In that case, we obtained less significant strain peaks. The wavenumber resolution was relatively low and a lower signal

[2] These measurements were performed with Emile Verstegen (Philips, Eindhoven), with courtesy.

was obtained from the strained-Si region. The penetration depth of the 454 nm laser in Si is around 300 nm, but due to the TiN and poly-Si layers on top of the Si, the signal could not be obtained from the whole strained Si volume. Therefore, although a laser with 532 nm wavelength had a high penetration depth, we got more signal from the Si fin compared to a laser with a 454 nm wavelength. Hence, for our analysis the 532 nm laser is a better choice.

Metallic tiles were on top of the FinFET structures. The metal layers were very thick and blocking the light. Therefore, they were removed using Focused Ion Beam (FIB) milling. Removal of these layers was necessary to obtain a good Raman signal from the area of interest. Fig. 2.7 shows the HR-SEM picture of a device before and after FIB removal of the metal layers. To prevent the damage to the stressor TiN layer, FIB process parameters were optimized at a 47 pA beam current and a process time of 5 minutes. A cross sectional SEM image after FIB processing confirmed that the stressor layer was still present. Raman spectroscopy on these samples was done by scanning the complete area of the channel region.

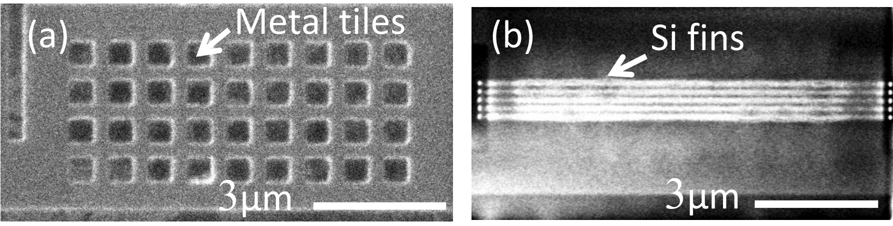


Fig. 2.7 HR-SEM image of a device before (a) and after (b) FIB removal of the metal layers.

Fig. 2.8 shows the peak map of the scanned device region before and after the FIB process. It is clearly observable that the Raman peak of the Si channel region is only detectable after the FIB process. To identify the Si channel from this map, the Raman peak at 520 cm^{-1} is highlighted. The contrast in this figure indicates different peaks of the Raman spectrum obtained from the channel. This map helps us to identify the Si fin region from the rest of the substrate and it was used for extracting the Raman spectrum of the strained channel region.

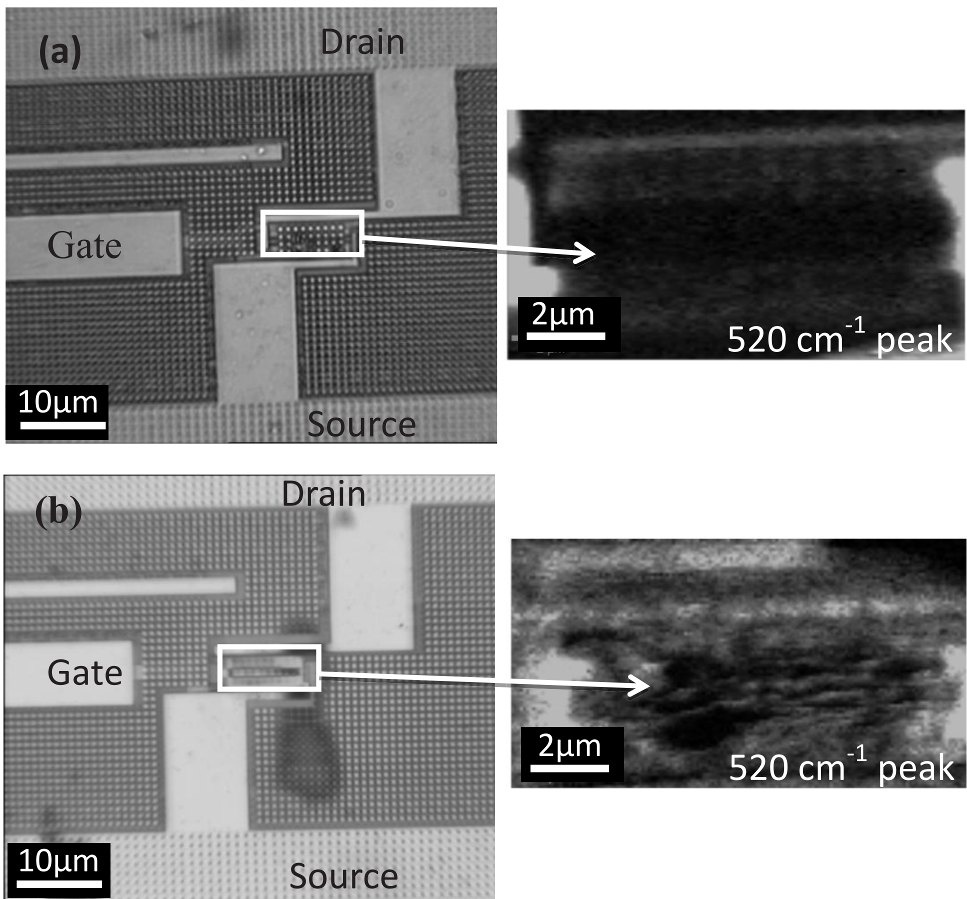


Fig. 2.8 Raman peak map of the channel region (a) before FIB, (b) after FIB preparation. The images on the right side show the peak position map of the Raman spectrum. The 520 cm^{-1} peak is highlighted with grey tones to identify the Si channel region from the BOX.

The devices with 10 µm gate length and different fin widths were used for measurements after FIB preparation. The samples have been analyzed by fitting the obtained Raman peaks with a Lorentzian function. The measurements are shown in Fig. 2.9.

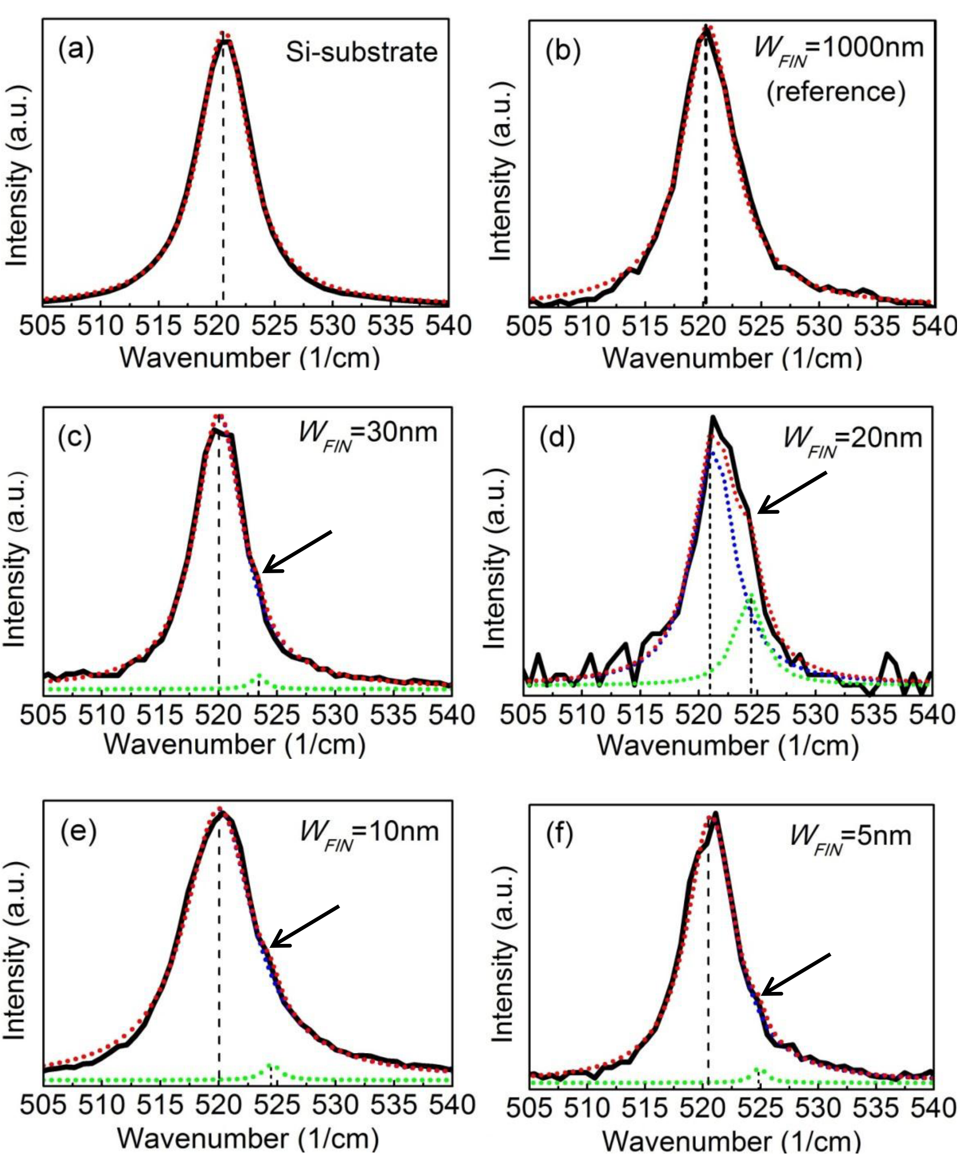


Fig. 2.9 Obtained Raman spectra of (a) the substrate, and that of the FinFET with a fin width of (b) 1000 nm, used as a reference, (c) 30 nm, (d) 20 nm, (e) 10 nm, (f) 5 nm. The blue dotted curves are the obtained Lorentzian fits corresponding to Si substrate. The green dotted curves are after fitting the second peak due to increased strain also indicated by the arrows to guide the eye. The total fits are indicated by red dotted curves.

In Fig. 2.9 (a) the Si substrate peak is shown. In Fig. 2.9 (b), the peak from the 5-fin FinFET device with W_{FIN}=1000 nm is presented. Since the Si-fin layer is only 60 nm thick and the penetration depth of the laser is larger than the sum of the Si fin and BOX layer thickness (≈ 340 nm), the substrate peak as well as the thin un-doped Si peak is present in the Raman spectrum. However, both Raman peaks are from Si and they appear almost at the same wavenumber without stress (i.e. 520 cm^{-1}). Therefore, it is not possible to differentiate them. This spectrum is used as a reference for strain calculations. Figs. 2.9 (c)-(f) show a second peak next to the substrate peak in the spectrum. The second peak is from the strained Si fin. It can be seen from Fig. 2.9 that the Si fin peak shifts to higher wavenumbers when the fin width is decreasing from 30 nm to 5 nm. The shift to higher wavenumbers is an indication of compressive stress [50]. Since the stress is much lower for the 1000 nm wide fin device, this second, stressed, Si peak cannot be observed. The first peaks are broadened because of the signal from the poly-Si layer on top of the fins [51]. The strained Si peak is weak compared to the substrate peak since the signal from the surroundings is 15-80 times bigger than that of the strained silicon fins. Therefore, for such a sample, it is quite difficult to get a significant signal from strained silicon but could still be used for the analysis.

The strain values were calculated from the Raman peak shift using the 1000 nm wide fin peak in Fig. 2.9 (b) as a reference. The calculations are dependent on the stress calibration using Raman shift data and the fitting of the peaks. In this way, the strain level and its evolution by fin width is provided. The strain was calculated using the Raman shift according to the following relations [51]:

$$\sigma = -250\,(MPa \cdot cm) \cdot \Delta\omega \qquad (2.2)$$

$$\varepsilon = \frac{\sigma}{E} \qquad (2.3)$$

where *E = Young's modulus,* σ *= stress,* ε *= strain,* $\Delta\omega$ *= peak shift.*

The Young's modulus of silicon along the z axis is taken as E_z =130 GPa [52] for the strain calculations. Table 2.2 shows the peak positions and calculated strain values for each device.

Table 2.2: *Strain values obtained from a Lorentzian peak fit.*

Fin width (nm)	Peak Position (cm^{-1})	Strain (%)
1000	520.3	reference
30	523.4	-0.60
20	524.2	-0.75
10	524.5	-0.80
5	524.9	-0.88

Fig. 2.10 shows the extracted strain values using the Raman shift data together with the strain values obtained by N. Serra *et al*. [37]. The authors used the holographic interferometry method on a similar set of devices to obtain strain information. The strain value obtained for W_{FIN}=10 nm with the Raman spectroscopy method is comparable to Serra's results while for W_{FIN}=20 nm our results indicates a larger strain value. The strain dependency on the fin width is clearly observed in both sets of data. Furthermore, Fig. 2.10 shows that the maximum strain values obtained from FEM simulations (see also section 2.3) agree well with the Raman spectroscopy data for a wide range of fin widths.

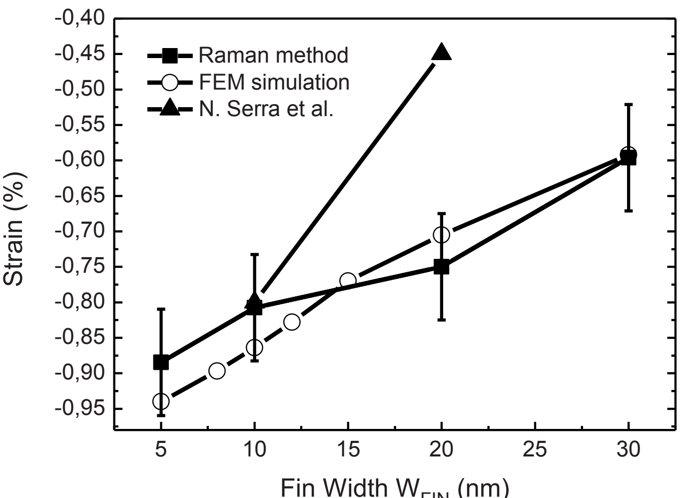


Fig. 2.10 Extracted strain values in silicon FinFETs using Raman spectroscopy. For comparison, FEM simulation and experimental data obtained from the holographic interferometry method [37] have been plotted in the same graph. Note that, due to the limitation of the Raman microscope system, the strain resolution is about 0.15 % for the Raman method.

2.3.2 Discussion

Compressive strain in Si fin height direction is known to move the Δ_2 valleys down, resulting in a decrease in the band gap of (110) oriented Si [9]. However, the band offset has never been experimentally studied in FinFETs. In section 2.3.1.1 the electrical measurements reveal that there is indeed a downward shift of the conduction band edge when the fin width is decreasing down to about 12 nm. Below this value, quantum confinement has a counteractive effect. In addition, the results obtained from optical measurements in section 2.3.1.2 show that strain is increasing for narrow fins. This is in line with the electrical data as well as holographic measurements and FEM simulations. Good agreement in the extracted strain values was obtained from Raman measurements FEM simulations and holographic interferometry. This indicates that Raman spectroscopy is a good method to obtain actual strain values in FinFET structures with nanometer dimensions. Furthermore, results obtained by these analyses can be used to explain the electrical measurements.

2.4 Conclusions

In this chapter, a brief introduction to strain, its use and methods in silicon-based devices, and its effect on band gap and mobility in solids is given. To characterize the strain at device level, temperature dependent *I-V* measurements and Raman spectroscopy technique were utilized for $(1\bar{1}0)/[110]$ oriented n-type strained FinFETs. Both techniques provided valuable information about the conduction band offset and strain level in a nanoscale device structure such as the FinFET.

The electrical results indicate that the conduction band energy offset, reaching values down to ≈ -40 meV, depends on the dimensions of the fin. This is explained by the superposition of two effects: (1) an increase in compressive strain in the fin height direction for smaller fins moving the Δ_2 valleys downward and (2) quantum confinement for fin widths below 12 nm, separating the energy levels available to electrons and moving the conduction band valleys upward.

A relatively small active device area of interest as well as high penetration depth causes a limitation for FinFET type device measurements with Raman spectroscopy. Despite this fact, reasonable results were obtained. It was shown that Raman peaks from Si fins shift to higher wavenumbers for narrow fins indicating compressive strain. Up to -0.88 % strain has been calculated from our Raman spectroscopy data. FEM simulations and holographic interferometry method were found to point out the same effect which leaded to the results obtained by electrical measurements. These are an indication that Raman

spectroscopy is an effective method to get strain information, even for small (nanoscale) regions of interest.

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3 Ferroelectric thin-film PZT layers

This chapter starts with a brief introduction to ferroelectrics and their applications. Then, the characterization of thin-film PZT/LNO stacks on an encapsulated TiN electrode is described for different stack layer thicknesses. Analysis of the electrical measurements indicates ferroelectric and piezoelectric properties and that a non-ferroelectric layer appears to be present at the PZT-electrode interface. The presented results in this chapter are important for the piezoelectric field-effect transistor (Chapter 5), in which these thin-film PZT/LNO layers have been integrated.

3.1 Introduction

Ferroelectricity is a property of a material that can reverse the spontaneous polarization by the application of an external electric field [1]. Ferroelectric materials also show piezoelectric properties. These materials generate a voltage when deformed by a mechanical force (*i.e.* piezoelectric effect) or physically changes in shape when a voltage is applied (*i.e. converse* piezoelectric effect).

Ferroelectric films attract much interest due to their applications in high density capacitors [2], sensors, micromechanical systems [3, 4] and nonvolatile memories [5, 6]. Recently, there have been a growing number of investigations on novel steep-subthreshold devices where thin ferroelectric or piezoelectric layers are employed. Salahuddin *et al*. [7] came up with a concept of using ferroelectrics as a gate dielectric to obtain a negative capacitance and hence improvement of the device properties. Later on, Rusu *et al*. [8] have demonstrated this concept experimentally on p-MOSFET devices. Their results show that it is possible to obtain a device with sub-threshold swing below the fundamental limit of 60 mV/dec at room temperature [9]. Newns *et al.* [10] proposed the piezoelectric transistor (PET) based on piezo-resistance effect on special channel materials manifesting a pressure-induced metal-insulator transition. They reported that the performance of PET's outpaces the conventional FETs with respect to the lower supply voltage and higher switching speed.

Another way to make use of the converse piezoelectric effect is to employ piezoelectric materials as a channel-stressor in a field-effect transistor. The application of stressors in Si technology was discussed in Chapter 2. So far, a piezoelectric stressor in a device structure has been proposed but not realized [11]. Simulations show that, if a proper strain configuration is formed, the sub-threshold swing (*SS*) can be decreased by ≈ 10 %. The strain distribution differs depending on the channel dimensions and the integrated materials. As demonstrated in Chapter 2, a large amount of strain can be obtained in narrow channels. This in combination with their strongly reduced short-channel effects makes FinFETs potentially attractive devices for integrating piezoelectric FETs (PiezoFETs). Lead zirconate titanate or PZT ($Pb[Zr_xTi_{1-x}]O_3$) is an attractive material for these applications, because of its relatively high piezoelectric response compared to other materials. PZT is a ceramic perovskite material and can be grown with different Zr to Ti concentration ratio that can change the properties. The PZT systems with a composition close to the morphotropic phase boundary (MPB, Ti/Zr=48/52) have high dielectric permittivity and piezoelectric response [12, 13]. The strong piezoelectric effect of these systems is attributed to the increased number of allowable domain states at the MPB [14]. Aluminum-Nitride (AlN) can be an alternative piezoelectric material to PZT, with

better CMOS compatibility and, however, a lower piezoelectric constant. It is also used in this work (see chapter 5).

The properties of PZT films are strongly dependent on the surrounding layers, the dimensions, and the fabrication conditions. Since the film/electrode interface becomes more prominent with scaling, thickness reduction may lead to reduced piezoelectric performance. In earlier works on scaling of PZT, small substrates and a buffer/electrode layer thicker than one hundred nanometer were used [15, 16]. These buffer/electrode layers were generally grown to relatively thick dimensions to keep control of the PZT growth orientation and to avoid ferroelectric performance degradation [17-19]. However, very thick PZT stacks are ineffective stressors due to the clamping effect [20].

The integration of ferroelectric/piezoelectric action in device structures could enable new functionalities. However, thick layer stacks do not meet the requirements for low-power, low voltage applications and are not compatible with the emerging technology [7, 10, 11, 15]. Uniform very thin films on large substrates are desired for the integration with nano-scaled devices in Si technology [8]. Therefore, there is a need for further research.

With this motivation, this chapter presents the analysis of thin-film $PbZr_{0.52}Ti_{0.48}O_3/LaNiO_3$ (LNO) stacks on the commonly used poly-Si/TiN gate stack for CMOS technology. LNO was used as a buffer layer and a diffusion barrier. TiN is a widely used material in advanced IC technology, due to the high temperature stability, mid-gap work function, low resistivity and good barrier properties [21]. The use of this material as a bottom electrode in PZT structures enables application of ferroelectrics in future Si technology nodes, such as a stressor for FETs [11]. Experimental results of the piezo-FinFET realized in the MESA+ Nanolab are presented in chapter 5.

3.2 PZT capacitors

3.2.1 Capacitor fabrication

Capacitor structures were realized on 100 mm Si wafers to characterize the thin PZT/LNO stacks. A schematic drawing of these structures is shown in Fig. 3.1. The processing started with a 5 nm TiN layer deposition on SiO_2 by atomic layer deposition (ALD). Subsequently, a 10 nm amorphous-Si layer was deposited without vacuum break by chemical vapor deposition (CVD) to prevent oxidation of TiN. This encapsulated TiN, a widely employed gate metal in advanced Si technology [21], was used as a bottom electrode for the PZT thin film capacitors. Then, the wafers were annealed at 900 ^{o}C for 30 seconds by rapid thermal annealing. As a result, the amorphous-Si layer is crystallized. As a buffer layer, LNO films of 5 nm, 10 nm and 20 nm thicknesses and homogeneous PZT films of 75 nm and 100 nm thicknesses were grown at 650 ^{o}C using a SolMateS large-area pulsed laser deposition (LAPLD) system. More information about the deposition process

can be found in ref. [22]. We kept the LNO buffer layer as thin as possible for the envisaged PZT properties. Finally, the PZT as well as the LNO film were patterned by wet etching by a 2 step process. Firstly, 5 sec in BHF (12.5 %):HNO_3:NH_4Cl:H_2O (8:1:8:32) at room temperature and secondly, 5 sec in HCl (45 %):H_2O (1:1) at 45°C. This 2-step process was repeated until the layer was completely etched. The first solution is an etching solution while the second one serves as a surface cleaner. After etching, a top electrode stack of 10 nm Ti and 100 nm Pt was sputtered through a shadow mask to fabricate 200 × 200 μm^2 capacitors [23]. Note that the resistivity of the encapsulated TiN layer was measured to be ≈ 160 μΩ-cm at room temperature (see chapter 4).

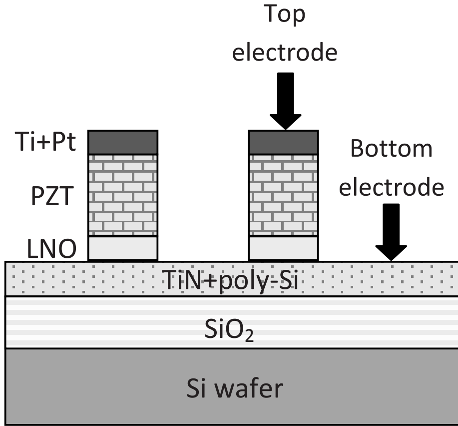

Fig. 3.1 Schematic drawing of the PZT capacitors. The dimensions are not to scale.

3.2.2 Characterization of the PZT stacks

3.2.2.1 XPS depth profile

X-ray photoelectron spectroscopy (XPS) has been used to obtain the compositional depth profile of the fabricated multi-film stack. XPS analysis is important to get information on the material distribution in different layers and on interfaces. It can detect diffusion of impurity atoms (e.g. Pb) into the silicon below the PZT/LNO stack. Impurity diffusion can degrade the performance of the underlying transistor.

Fig. 3.2 (a) shows the XPS depth profile in a capacitor. Starting from the surface, metallic layers of Pt and Ti are recognized in the XPS depth profile. Then, after about 6 minutes of sputtering, the PZT layer is reached. Below that layer the LNO, poly-Si and TiN layers can be observed. Fig. 3.2 (b) shows a magnification of the PZT-Si-TiN-SiO_2 interface region. No diffusion of Pb in the Si layer is observed within the resolution limit of XPS (≈ 0.5 at. %). This implies that, when deposited on FinFETs, no degradation of the transistor properties is expected.

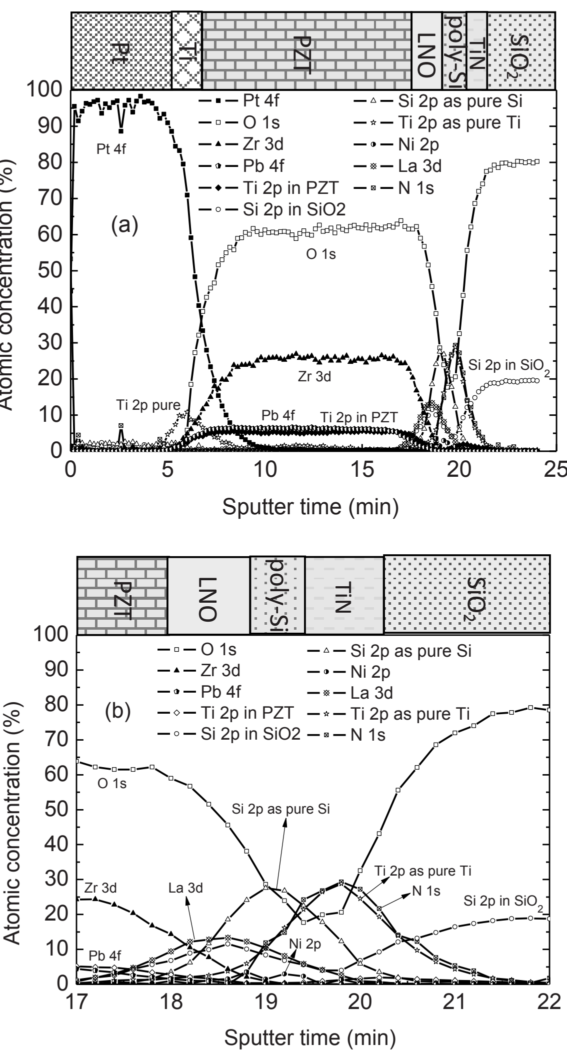

Fig. 3.2 XPS depth profile of the PZT capacitor (a) from top to SiO_2 layer, (b) magnified PZT-LNO-poly-Si-TiN-SiO_2 stack. The layer stack is schematically drawn on top of the graphs to guide the eye.

3.2.2.2 XRD analysis

Ferroelectric film properties are both affected by orientation and crystallinity. X-ray diffraction (XRD) analysis is typically used for analyzing the crystalline properties of the material/film. For instance, Tsukada *et al.* [24] demonstrated that if the volume fraction of (001) orientation in the (001)/(100)-oriented films is high the switchable polarization will also be high. Since the polarization direction is easily aligned to the c-axis (001) in tetragonal PZT, this orientation could give higher polarization. Furthermore, Nagashima *et al*. [25] reported that the Zr/Ti ratio influences the crystal orientation dependence of the ferroelectric properties.

The XRD spectra of the 100 nm and 75 nm thick PZT films on different LNO thicknesses are shown in Fig. 3.3 (a) and (b). These spectra show a typical perovskite polycrystalline PZT structure without preferred orientation. Except for 5 nm LNO, both (100)/(001) and minor (110)/(101) orientations are observed. However, a 60 nm PZT film showed only a weak (100)/(001) XRD peak (data not shown). Since our samples show major (100)/(001) orientations, we expect that these films have good ferroelectric properties.

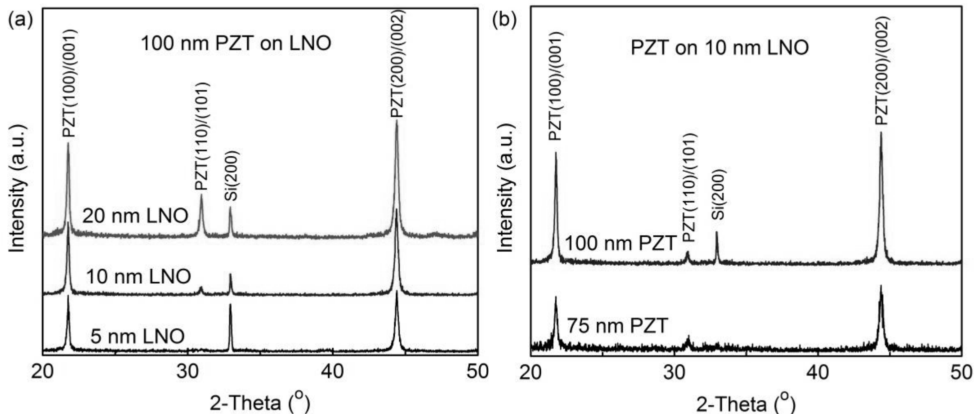

Fig. 3.3 XRD graphs of (a) a 100 nm-thick PZT film on different LNO layer thicknesses and (b) a 75 nm and a 100 nm PZT film on a 10 nm-thick LNO layer.

3.2.2.3 Laser Doppler vibrometer measurements

A Polytec MSA-400 Micro-scanning laser Doppler vibrometer (LDV) tool was used in this study. The LDV method is utilized for non-contact measurement of surface vibrations [26, 27]. A schematic set-up of an LDV system is shown in Fig. 3.4. The laser beam reaching the surface is reflected by the sample and detected by a measurement system. From the Doppler shift of the laser beam frequency, the amplitude and frequency of the surface vibrations can be obtained.

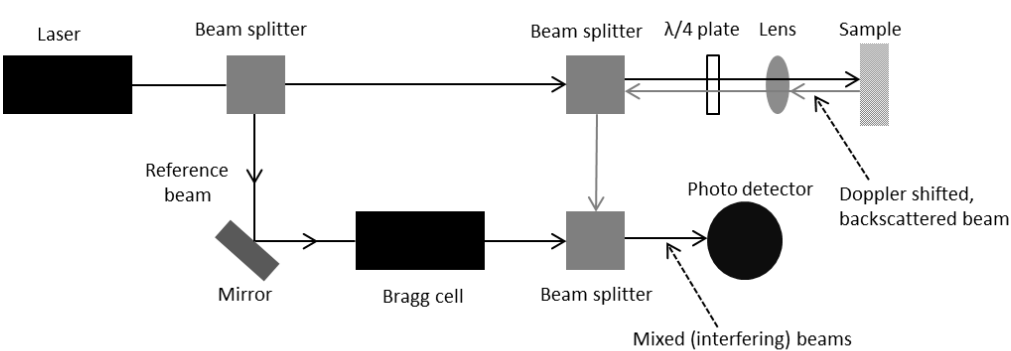

Fig. 3.4 Schematic set-up of the LDV system

In the measurement system, the He-Ne laser (λ=632.8 nm) beam is split by the first beam splitter into a reference beam and a measurement beam. The measurement beam passes through a second beam splitter and focuses on the object or sample. The object reflects the beam and the beam deflects towards a second beam splitter. In the meantime, the reference beam passes through the Bragg cell, which gives a frequency shift. The measurement beam and the reference beam are merged by a third beam splitter and then directed onto a photo detector. The superposition of the reference and the measurement beam generates an interference pattern. As the path length of the beam is constant over time, dark and bright fringes are generated. One complete dark-bright cycle corresponds to the displacement of a half of the laser wavelength (in case of the He-Ne laser, this is around 316 nm). The change in the path length per unit time corresponds to a Doppler shift of the beam. The velocity of the object can be directly determined by the modulation frequency of the interferometry pattern. If the sample generates the same pattern while moving forward and backward, the direction of the pattern cannot be determined without the help of a Bragg cell. The Bragg cell shifts the light frequency by 40 MHz and enables detecting upward and backward motion [28].

In this study, the effective piezoelectric coefficient ($d_{33,f}$) was determined using the laser Doppler vibrometer (LDV) method with a resolution in the pm range [28]. The piezoelectric capacitor was excited by applying a 1 V dc-voltage and a sinusoidal ac-voltage of 2 V at 8 kHz frequency at the top electrode. The response under these measurement conditions is shown in Fig. 3.5 (a) for an upward displacement. From the line scan profile in Fig. 3.5 (b) a maximum $d_{33,f}$ coefficient is calculated as δ_{top}/V_{ac}=53 pm/V. This value is very close to reported values obtained from relatively thick PZT layers (800 nm) [29]. When the PZT film is used for steep sub-threshold devices, it is crucial to have films with a high $d_{33,f}$ value [11]. Similar $d_{33,f}$ values were obtained for a 75 nm thick PZT film.

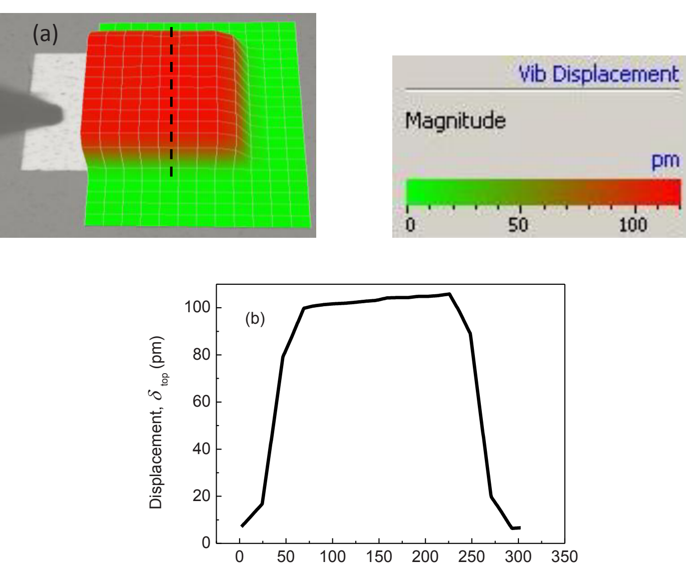

Fig. 3.5 (a) 3D upward response scan of the two dimensional piezoelectric layer. A 1 V dc and a 2 V ac voltage at 8 kHz frequency was applied to the film. (b) A line scan profile of the piezoelectric displacement of top electrode across the dashed line. The piezoelectric coefficient is $d_{33,f}$ =53 pm/V. Note that a 20 nm LNO + 100 nm PZT stack was used in this experiment.

3.2.3 Electrical and ferroelectric characterization

3.2.3.1 Polarization hysteresis measurements

The polarization hysteresis loop measurement is an indicator of the ferroelectric behavior of the material. The measurements in this work were carried out by using an aixACCT Analyzer TF2000[1]. The polarization hysteresis (*P-E*) loops of the PZT capacitors for an LNO layer thickness of 10 nm and 20 nm are shown in Fig. 3.6. No change in remnant polarization (P_r) is observed when the LNO thickness is decreased from 20 nm to 10 nm. However, for an LNO thickness of 5 nm, the P_r drops abruptly (data not shown). Therefore, in this study, the LNO layer thickness was kept at the minimum of 10 nm for all PZT samples. For the 100 nm and 75 nm thick PZT layers, average P_r values of 19 μC/cm^2 and 18 μC/cm^2 are obtained, respectively. The average coercive field is approximately 200 kV/cm. The *P-E* loops show offsets both in the field and in the polarization axis. A possible explanation will be discussed in the next section.

[1] The measurements were performed at the Inorganic Materials Science group (MESA+ Research Institute for Nanotechnology, University of Twente, The Netherlands.)

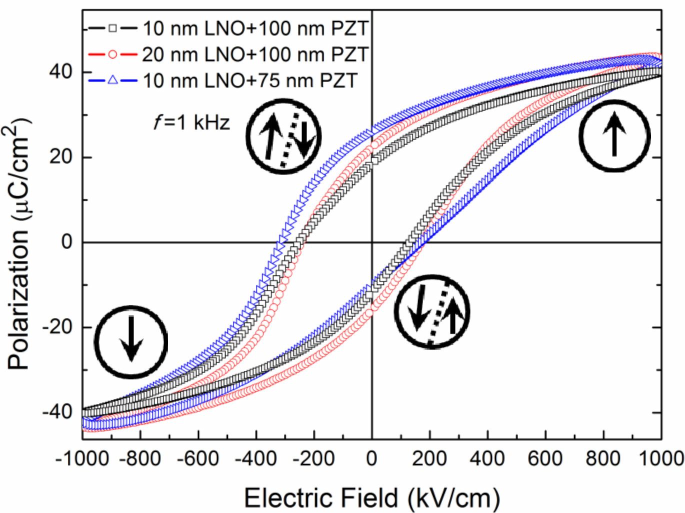

Fig. 3.6 Thickness dependence of polarization hysteresis (P-E) loops. The P-E loops were performed at an applied ac-electric field of ±1000 kV/cm and 1 kHz frequency. The arrows indicate the polarization state of the material at the indicated fields. The bottom electrode was grounded and a maximum dc bias of 10 V was applied to the top electrode (see Fig. 3.1).

3.2.3.2 *C-E* and *J-E* measurements

The electrical performance of the PZT layer in terms of leakage current and capacitance is also of major importance for device applications. Capacitance-electric field (*C-E*) and temperature dependent leakage current density-field (*J-E*) measurements were performed using a SÜSS Microtech probe station equipped with a Keithley 4200 semiconductor characterization system. Fig. 3.7 shows the dielectric constant-electric field curves obtained from the capacitance measurements of the 75 nm and 100 nm thick PZT films. The dielectric constant was obtained from the *C-E* measurements at an ac bias of 30 mV and a switching frequency of 1 kHz.

We observe a typical butterfly shaped hysteresis in the dielectric constant versus electric field curves. This is a ferroelectric behavior and indicates the domain re-orientation process inside the PZT layer [30, 31]. However, as observed in the polarization loop experiments, the center of the hysteresis loops has shifted towards the negative bias range. In addition, there is an asymmetry in the maximum dielectric constant values, especially for the capacitor with a 75 nm-thick PZT layer. The shift in hysteresis loops as well as the asymmetry in the dielectric constant could be due to space charge accumulation at the PZT/electrode interface. This can be seen as an additional non-ferroelectric or passive layer adjacent to the electrodes, which could have been formed during the fabrication of the capacitor stack [32-37].

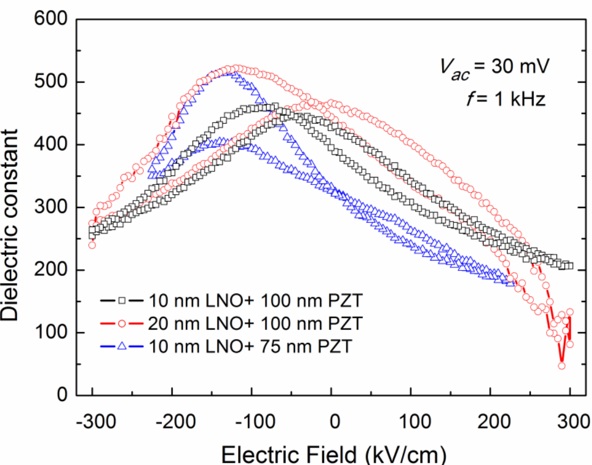

Fig. 3.7 Dielectric constant-electric field curves of the PZT capacitors for various LNO layer and PZT film thicknesses (f =1 kHz, V_{ac}=30 mV). The bottom electrode was grounded and a maximum dc bias of 3 V was applied to the top electrode.

Generally, this passive layer can form (*i*) a graded junction, (*ii*) an insulating defect layer, (*iii*) an intermediate compound/phase or (*iv*) a highly charged layer inside the PZT capacitor [38]. Therefore, the term "effective" is used to describe its properties. This layer can affect both ferroelectric and piezoelectric properties. Such a thin layer could be more prominent when the thickness of the PZT layer decreases, which can explain the thickness dependence of the difference in the maximum dielectric constants.

The problem, as will be shown further in section 3.2.3.3, is that the location is uncertain and the physical thickness of the passive layer is too thin to be detected by any optical or electron-beam technique. Therefore, in our analysis, we assume a single passive layer in the PZT capacitor which is assumed to be present at the Ti/PZT interface. This is because the PZT/LNO interface received a higher temperature treatment than the top Ti/PZT interface, resulting in less extended structural defects for the former [39]. Note that this is one possible way to explain the system. As will be shown later, it is based on a working hypothesis.

3.2.3.3 Analysis

There have been several reports in which the passive layer properties were estimated for different ferroelectric materials [35, 40]. These have been reported for PZT by M. D. Nguyen [22]. To obtain the dielectric constant of the PZT layer, as well as the properties of the passive layer, the following series capacitor equation is employed [40]:

$$\frac{1}{C_{total}} = \frac{1}{C_{pass}} + \frac{1}{C_{PZT}} = \frac{1}{A\varepsilon_0}\left(\frac{t_{pass}}{\varepsilon_{pass}} + \frac{t_{PZT}}{\varepsilon_{PZT}}\right) \quad (3.1)$$

where, ε_0(=8.85×10^{-12} F/m) and ε_{PZT} are the vacuum permittivity and relative dielectric constant of the PZT layer, respectively. ε_{pass} is the relative dielectric constant of the passive layer between film and electrode and *A* is the capacitor area, t_{PZT} and t_{pass} are the thickness of PZT ferroelectric film and the effective thickness of the passive layer, respectively.

Assuming a relatively thin passive layer thickness, the effective values of relative dielectric constant ε_{PZT} and $t_{pass}/\varepsilon_{pass}$ are calculated from the inverse capacitance vs. PZT layer thickness (1/*C*-t) graph. The 1/*C*-*t* curve obtained at zero volt is shown in Fig. 3.8. From the slope and the intercept values of this curve, the effective values of the relative dielectric constant ε_{PZT} and $t_{pass}/\varepsilon_{pass}$ are calculated to be 600 and 8.95×10^{-11} m, respectively.

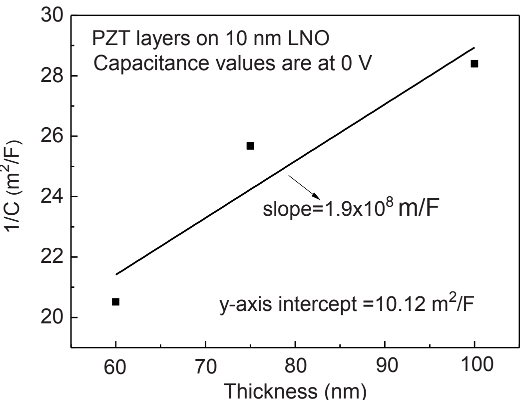

Fig. 3.8 1/*C* vs thickness curve at zero volt bias. The LNO layer was 10 nm thick for all samples.

Additional information on the passive layer is obtained from leakage current density-electric field (*J*-*E*) measurements on the PZT capacitors. Unfortunately, during the PLD process, large clusters of the target material were also deposited. This resulted in an inhomogeneous film and consequently non-uniformly distributed paths in the leakage current. Therefore, the leakage current of the capacitors depends also on these additional leakage paths.

Several capacitors were tested in this work and the ones with a relatively low leakage are plotted. Fig. 3.9 shows the *J*-*E* characteristics of the capacitors at room temperature. It is

observed that the thicker LNO layer gives a lower leakage. This could be due to the growth of a higher quality PZT material.

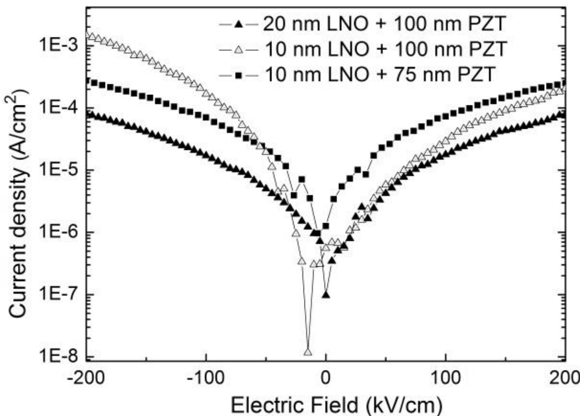

Fig. 3.9 Room temperature *J-E* characteristics of a 75 nm and a 100 nm PZT film on a 10 nm-thick and 20 nm-thick LNO layer.

The Ti and the LNO that contact the PZT layer have a work function of 4.33 eV [41] and 4.60 eV [42], respectively. Since the electron affinity of PZT is around 3.5 eV [38], we expect an asymmetry due to the 0.27 eV difference in Schottky barrier height (SBH) between top and bottom contacts for the 'ideal' PZT capacitor. The minimum SBH would be that at the Ti/PZT interface: 0.83 eV. However, the *J-E* curves are almost symmetric for forward and reverse biases. This behavior can be attributed to the existence of interface states at the contacts, resulting in barrier alignment [43], yielding symmetric *J-E* curves.

Furthermore, in our work, the PZT layer is intentionally undoped and relatively thin, meaning that the electrodes govern the electrostatics. To see the effect of doping in the band alignment of PZT structure, TCAD (technology computer aided design) simulations [44] were performed[2] as shown in Fig. 3.10.

Since the differences between the electron affinity of PZT and the work functions of Ti and LNO are relatively low compared to half the band gap of PZT (E_G=3.2 eV), the leakage current of the PZT system under study is an electron current, *i.e.* n-type conduction.

[2] Simulations were performed by R.J.E. Hueting, with courtesy.

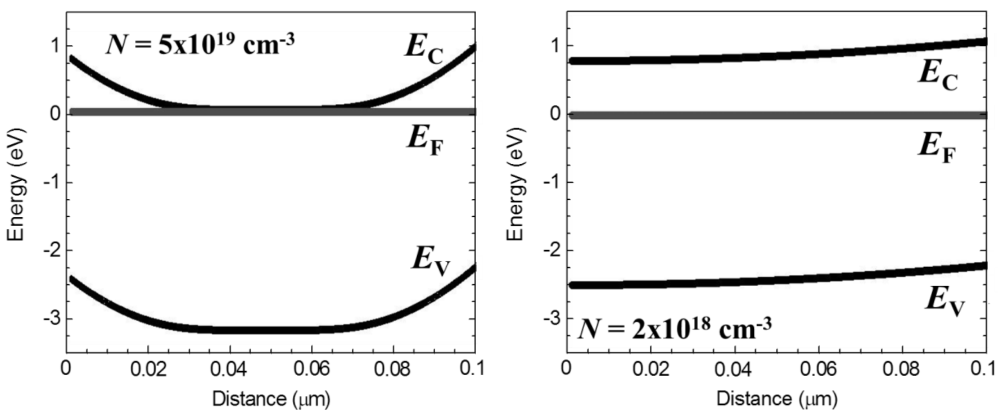

Fig. 3.10 The energy band diagram of the 100 nm thick PZT layer with (a) 5×10^{19} cm^{-3} and (b) 2×10^{18} cm^{-3} doping. The Ti/PZT interface (left) and PZT/LNO interface (right) give a barrier height of 0.8 and 1.1 eV, respectively.

By inserting the experimental layer thickness and low doping level (less than 2×10^{18} cm^{-3}), a full depletion of the PZT layer was predicted by the simulator. Therefore, although linear behavior of the ln *J*-$\sqrt{E}$ graph in our capacitors (not shown) indicates Schottky type emission, it is questionable whether the current conduction can be explained by pure Schottky emission. This is because of fully depleted layers comprising a passive layer at the interface with almost symmetric *J-E* curves. In addition, as will be shown later in Fig. 3.11, the weak temperature dependence of the current density is an indication that the SBH is lower than expected.

Based on the diffusion theory in metal-semiconductor contacts [9], it can be derived from the drift-diffusion equations that:

$$J = qN_C\mu_n u_T\left[exp\left(\frac{V}{u_T}\right) - 1\right] / \int_0^t exp\left[\frac{E_C(x)}{kT}\right]dx\,, \text{ with} \qquad (3.2)$$

$$N_C = 2\left(\frac{2\pi m_{eff}kT}{h^2}\right)^{3/2},$$

where T is the temperature, q is the elementary charge, t is the total layer thickness, μ_n is electron mobility, u_T is thermal voltage ($=kT/q$), k is Boltzmann's constant, N_C is the conduction band effective density of states, m_{eff} is the effective mass, h is Planck's constant, and $E_C(x)$ is the conduction band energy depending on the distance x.

Using Eq. (3.2) for an ideal asymmetric metal-ferroelectric-metal structure in full depletion mode, we obtain:

$$J = qN_C\mu_n\left(\frac{\varphi_{B1}-V-\varphi_{B2}}{t_t}\right)\frac{exp\left(\frac{V}{u_T}\right)-1}{exp\left(\frac{\varphi_{B1}}{u_T}\right)-exp\left(\frac{\varphi_{B2+V}}{u_T}\right)}\ , \qquad (3.3a)$$

where φ_{B1} and φ_{B2} are the barrier heights at the Ti/PZT and PZT/LNO interfaces, respectively. Depending on the differences in the barrier heights, the reverse and forward current will be different. In Fig. 3.11, the current density is plotted against the applied voltage showing that the model (Eq. (3.3a)) is in good agreement with TCAD simulations. The results also show a large asymmetry in the *I-V* curve for a positive and a negative bias.

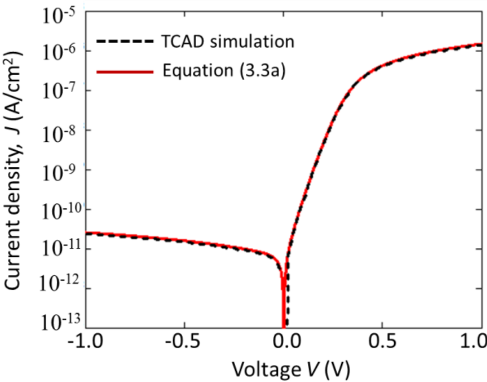

Fig. 3.11 *J-V* graph of the PZT capacitor structure obtained from TCAD simulations and from the model (Eq. 3.3a).

As stated before, the barrier heights seem to be almost equal, φ_{B2}=φ_{B1}=φ_B, possibly due to interface states. From Eq. (3.3a) we can see that for this case the equation reduces to:

$$J = qN_C\mu_n\left(\frac{V}{t_t}\right)exp\left(-\frac{\varphi_B}{u_T}\right). \qquad (3.3b)$$

This equation shows a weak voltage dependency and is symmetric. However, the image force lowering effect is primarily present at the interface, and the passive layer is not included here. This affects the integral of the conduction band energy, see Eq. (3.2). Therefore, the following leakage current equation, developed by Simmons, applies for PZT capacitors [38, 45]:

$$J = \underbrace{2q\left(\frac{2\pi m_{eff}kT}{h^2}\right)^{3/2}\mu E}_{K(V)=\alpha V}\ exp\left(-\frac{\varphi_B}{u_T}\right)exp\left(\sqrt{\frac{qE_{pass}}{4\pi\varepsilon_0\varepsilon_{pass}}}/u_T\right), \qquad (3.4)$$

where φ_B is the SBH, ε_0 is vacuum dielectric constant, ε_{pass} is the dielectric constant of the passive layer, and E is the applied field across the PZT layer. This model is comparable with Eq. (3.3b); however, it has an additional exponential term. This exponential term determines the charge injection at the electrode-ferroelectric interface and E_{pass} represents the field at the interface. Eq. (3.4) describes that the injection is interface-controlled, while the transport is a bulk-controlled phenomenon, i.e. diffusion, governed by the integral of the potential barrier over the PZT film thickness.

The properties of the passive layer can be found using Eq. (3.4), where the slope of the ln J-$\sqrt{V}$ graph is equal to $q\sqrt{q/4\pi\varepsilon_0\varepsilon_{pass}t_{pass}}/kT$. This method has been used before in other studies using the pure Schottky emission equation [35, 40]. However, in this case $V = V_{pass}$, the voltage drop across the passive layer, and the relation between V and V_{pass} needs to be determined. This relation can be found by writing the electric displacement at the PZT film-passive layer interface. The electric displacement in PZT can be described as $D = \varepsilon E$ by assuming that the polarization of the material is linearly dependent on the field, which holds especially at low fields. At a boundary between the passive layer and PZT film, the displacement field is continuous, i.e. $\varepsilon_{PZT} E_{PZT} = \varepsilon_{pass} E_{pass}$.

Therefore, V_{PZT} can be written as:

$$V_{PZT} = \varepsilon_{pass}V_{pass}t_{PZT}/(\varepsilon_{PZT}t_{pass}). \quad (3.5)$$

The applied voltage is the sum of the voltage drop over the passive layer and over the PZT ($V = V_{pass}+V_{PZT}$). Since ε_{PZT} = 600 and $t_{pass}/\varepsilon_{pass}$= 8.95×10^{-11} m, V can be estimated to be 2.86×V_{pass} from Eq. (3.5). The slope of ln J-$\sqrt{V_{pass}}$ curve is 6.74 and hence $t_{pass}\varepsilon_{pass}$ = 47.26 nm. Therefore, employing capacitance and leakage current measurements, the effective passive layer thickness and its relative dielectric constant are estimated to be 2.1 nm and 23, respectively. Such a thin passive layer is difficult to observe with any physical technique. Moreover, the effective electrical thickness might be different from the actual physical layer thickness.

The SBH can be extracted from temperature dependent current density – electric field (J – E) measurements. Fig. 3.12 shows the temperature dependent leakage characteristics of capacitors with 60 nm, 75 nm and 100 nm thick PZT layers.

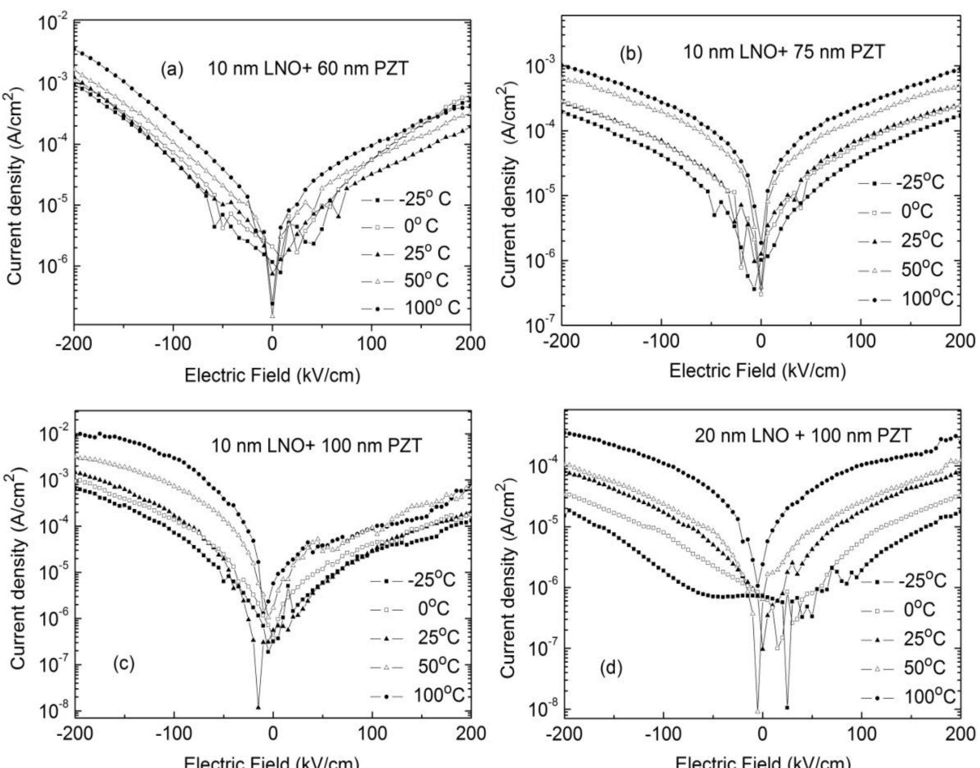

Fig. 3.12 Temperature dependent *J-E* characteristics of (a) a 60 nm (b) a 75 nm (c) a 100 nm PZT film on a 10 nm-thick LNO layer and (d) a 100 nm-thick PZT film on a 20 nm thick LNO layer.

The temperature dependency of the leakage current is different for each sample. A weak temperature dependency is observed, especially for thin PZT layers. The sample with the lowest leakage and a $T^{3/2}$ temperature dependency, presented in Fig. 3.12 (d), was chosen for the SBH extraction.

For this purpose, $\ln(J/T^{3/2})$ curves have been plotted against $1/T$ in Fig. 3.13 (a) for different constant forward bias voltages. The slope of these curves equals to $-q\left(\varphi_B - \sqrt{qE_{pass}/4\pi\varepsilon_0\varepsilon_{pass}}\right)/k$. Inserting the parameters we calculated before, we obtain for the SBH at the Ti/PZT interface $q\varphi_B$= 0.32 eV. As mentioned before the expected minimum SBH would have been around 0.8 eV. The measured low (apparent) barrier height however can be attributed to ferroelectric polarization induced barrier lowering as reported by Pintilie *et al*. [39].

Fig. 3.13 (b) and Fig. 3.13 (c) show the measurements of the current density as a function of the applied electric field (symbols). The solid lines represent theoretical fit using Eq. (3.4), keeping the factor α of the voltage dependent pre-exponential term $K(V) = \alpha V$ as a fitting parameter. This parameter (α) is in the same order as reported by Pintilie *et al.*

[39], i.e. 10^{-5}A/Vcm^2. Hence, there is a good agreement between the measurements and the theoretical fit both for reverse and forward bias conditions. Therefore, the barrier heights for bottom and top interfaces are the same in our 20 nm LNO + 100 nm PZT capacitor structures.

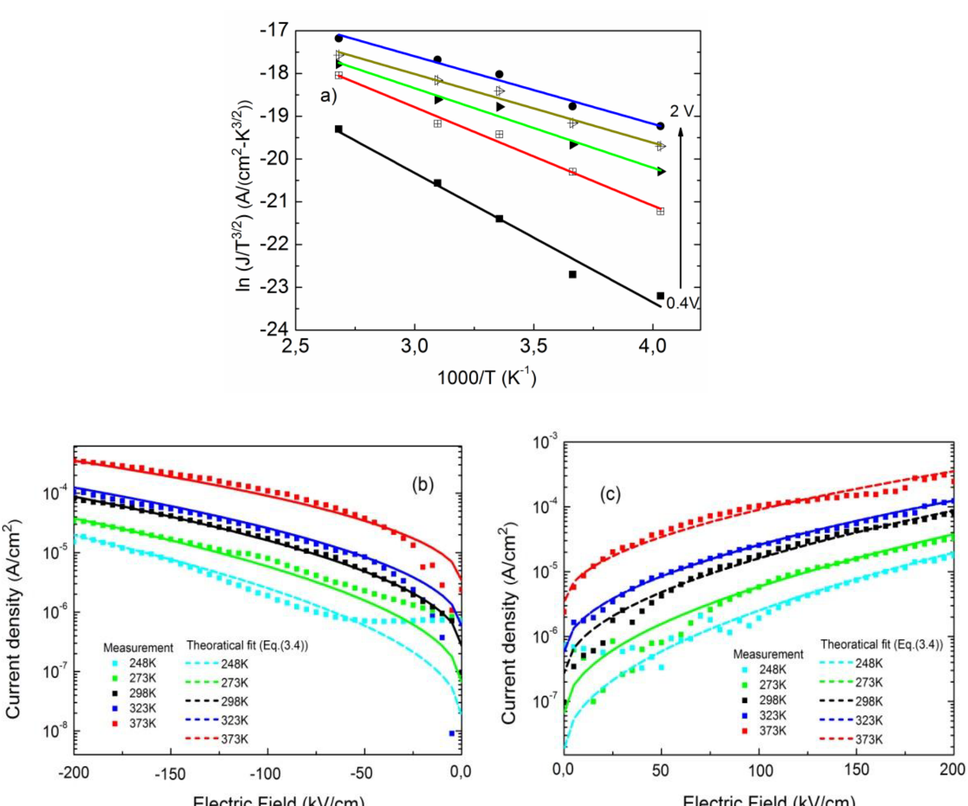

Fig. 3.13 (a) ln ($J/T^{3/2}$) plotted against $1/T$ for different constant forward bias voltages, (b) and (c) measured *J-E* curves (symbols) and theoretical fit (dotted lines) for 20 nm LNO + 100 nm PZT film for different measurement temperatures at reverse and forward bias, respectively.

3.3 Conclusions

In this chapter, thin-film PZT/LNO stacks with different layer thicknesses deposited on an encapsulated TiN electrode were studied. XRD analysis evidenced (100)/(001) and (110)/(101) orientations of the PZT layer and the results obtained from the XPS analysis show no significant diffusion of atoms between the different layers, which is important for the device behavior. We obtained a promising effective piezoelectric coefficient $d_{33,f}$ reaching a maximum value of 53 pm/V. The high $d_{33,f}$ value favors PZT as a stressor for device structures like steep sub-threshold switches. In addition, an average remnant

polarization P_r of 19 μC/cm^2 is obtained. A shift in the *P-E* hysteresis loops as well as an asymmetry in the dielectric constant against the electric field was observed.

Based on the electrical analysis, the properties of the 100 nm thick PZT layer and PZT-electrode interface were determined. Although a 0.27 eV difference in SBH between top and bottom contacts is expected for the 'ideal' PZT capacitors, the *J-E* curves obtained from thin-film PZT capacitors are almost symmetric for forward and reverse biases. Together with a shift and an asymmetry mentioned before, this effect can be an indication of an additional non-ferroelectric or passive layer adjacent to the electrodes. This layer can result in barrier alignment and yield symmetric *J-E* curves.

Further analysis was done by capacitance and leakage current measurements to obtain dielectric properties of PZT and passive layer. It is found that the relative dielectric constant of the PZT layer has a value of 600 whereas the effective thickness and the relative dielectric constant of the passive layer are estimated to be 2.1 nm and 23, respectively. In addition, a low apparent barrier height of 0.32 eV was obtained, possibly due to ferroelectric polarization induced barrier lowering.

The obtained values have been inserted into the leakage current equation and good fitting has been obtained between the measurements and the model (see Fig. 3.13 (b) and (c)). Therefore, our analysis on sub-100 nm PZT layers shows that the leakage current can be described with a diffusion-based rather than a pure Schottky emission model. Furthermore, the leakage current is governed by interface controlled injection and its transport is diffusion-limited.

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4 Fabrication and characterization of FinFETs

This chapter presents a fabrication scheme of FinFET devices realized at the MESA+ Research Institute, Twente. The devices and the process control test structures were characterized both electrically and optically. It is shown that the fabricated FinFETs have a well-defined body down to 20 nm wide dimensions and an aspect ratio up to 7.5. The functional devices show promising performance with near-ideal sub-threshold swing (≈ 75 mV/dec) and high on-current off-current ratio I_{on} / I_{off} of around 10^8. *The devices presented in this chapter pave the way for the novel steep sub-threshold devices, discussed in Chapter 5.*

4.1 Fabrication of FinFETs

4.1.1 Design

FinFETs consist of fins, S/D areas and metal contacts. Because of improved gate control (see section 1.2), FinFETs with sub-tens of nanometer fin width (W_{FIN}) are desired. The devices designed in this work comprise fin widths from 15 nm to 1000 nm. To process these aggressive dimensions as well as features in micron range for contact regions, both an electron beam system (the Raith 150-TWO) and optical contact lithography was used.

Devices with different number of fins, W_{FIN} and gate length (L_{gate}) were designed with the Cadence mask design software. Fig. 4.1 shows the schematic mask layout of a typical FinFET including its design parameters. All the designed devices comprise either a single fin or 5 parallel fins. The designed pitch for the FinFETs is 1 µm except for the 1 µm wide devices having a pitch of 3 µm. Source-Drain extensions (L_{sd}) were designed as 15-23 µm long. An overview of the designed mask dimensions is given in Table 4.1.

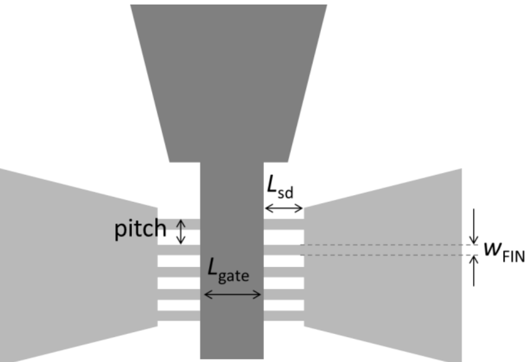


Fig. 4.1 Schematic mask layout of the FinFET with its design parameters.

Table 4.1 *Summary of the designed FinFET mask dimensions*

	W_{FIN}	W_{FIN}	W_{FIN}	W_{FIN}	W_{FIN}	W_{FIN}	W_{FIN}	W_{FIN}
L_{gate} =2 µm	15 nm	20 nm	30 nm	40 nm	50 nm	60 nm	100 nm	1000 nm
L_{gate} =3 µm	15 nm	20 nm	30 nm	40 nm	50 nm	60 nm	100 nm	1000 nm
L_{gate} =10 µm	15 nm	20 nm	30 nm	40 nm	50 nm	60 nm	100 nm	1000 nm
L_{gate} =20 µm	15 nm	20 nm	30 nm	40 nm	50 nm	60 nm	100 nm	1000 nm
L_{gate} =30 µm	15 nm	20 nm	30 nm	40 nm	50 nm	60 nm	100 nm	1000 nm

Process control test structures were also designed for specific purposes. The Greek Cross (GC) structure [1] is commonly used to measure the sheet resistance of the layers. In this

GC structure, the current (I) is forced between two nearby positioned contacts and the voltage drop (V) over the central square is measured using the other two contacts (see e.g. Fig. 4.2). The measured resistance (R) is V/I. If $L > 2W$, the size and shape of the contacts does not have an effect on the potential distribution and the structure fulfill the Van der Pauw boundary conditions. A correction factor $\pi/\ln(2)$ is used to extract sheet resistance (R_{sh}) [1-3]. Therefore,

$$R_{sh} = \frac{\pi}{\ln(2)} R. \tag{4.1}$$

As shown in Fig. 4.2, the GC structures were used for three different purposes in this work: to determine *i*) the doping concentration in the S/D extension regions from the resistance measurement, *ii*) the sheet resistance of the gate material, and *iii*) the sheet resistance of the channel. In Fig. 4.2 (a), the GC composed of two doped-Si arms. This structure was used to address point *i*). In Fig. 4.2 (b), both arms of the structure compose gate layers (poly-Si/TiN) to measure the sheet resistance of the gate material (point *ii*)). Fig. 4.2 (c) shows the GC with one arm Si and the other arm gate material. During processing, this structure faced the same treatment as the FinFETs. Therefore, the Si under the gate is supposed to be undoped whereas the rest of Si arm is doped like the S/D extensions. Using this test structure, the channel resistance can be measured to identify whether the masking was successful in keeping the channel un-doped. Table 4.2 shows the width (W) and length (L) dimensions of the GCs.

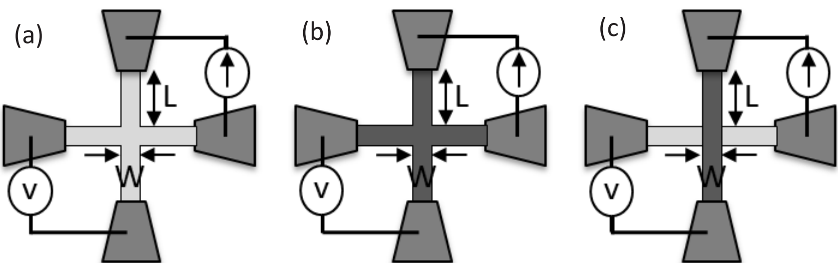


Fig. 4.2 The GC structure comprising (a) doped Si arms (GC I) (b) poly-Si/TiN arms (GC II) (c) a Si arm (light grey) crossing with a poly-Si/TiN (dark grey) arm, as in the FinFET (GC III). The figures are not to scale.

Table 4.2 *W* and *L* *dimensions of the GC test structures used for the design*

	W **of lateral × vertical arm**	***L*** **of lateral × vertical arm**
GC (I)	100 nm × 100 nm	25 µm × 15 µm
	1 µm × 1 µm	25 µm × 15 µm
GC (II)	5 µm × 5 µm	25 µm × 15 µm
	10 µm × 10 µm	25 µm × 15 µm
GC (III)	100 nm × 5 µm	25 µm × 15 µm
	1 µm × 10 µm	25 µm × 15 µm

A commonly used structure to characterize Si-metal contacts is the Cross Bridge Kelvin Resistor (CBKR), as shown in Fig. 4.3 [1, 4, 5]. The measurement principle is forcing a current (I) between pads 1 and 2 and measure the voltage drop (V_{34}) between pads 3 and 4. The Kelvin resistance R_k can be found as:

$$R_k = \frac{V_{34}}{I}\,. \qquad (4.2)$$

To obtain the specific contact resistance (ρ_c), a 2D-Model needs to be applied since there is an overlap δ>0 (see Fig. 4.3). This results in a lateral current flow around the contacts leading to an additional voltage drop, which results in a higher Kelvin resistance [6, 7]. In this model, the measured R_k is then a result of the current through and around the contact. According to the model, ρ_c can be calculated using Eq. (4.3):

$$R_k = \frac{\rho_c}{A} + \frac{4R_{sh}\delta^2}{3W_xW_y}\left[1 + \frac{\delta}{2(W_x-\delta)}\right] \qquad (4.3)$$

where R_{sh} is the sheet resistance of the overlapping of the underlying Si layer. The other structure parameters are shown in Fig. 4.3.

The CBKR structure was defined in the same way as Si fins (see section 4.1.2). After the cross was defined, gate oxidation was done and TiN and α-Si layer were deposited as gate layers. Gate etching was done, leaving a contact hole in the center of the cross, as shown in Fig. 4.3. Afterwards, S/D implantation and activation was done. The lift off mask was defined and the gate oxide was removed to prepare the contact holes for the metallization. After Al-Si deposition, the lift off process was done (for further details see section 4.1.2). The dotted area in Fig. 4.3 indicates the metallic layer. Square contact holes show the region where the actual metal-Si contact is. The dimensions of the structure are also shown in the inset.

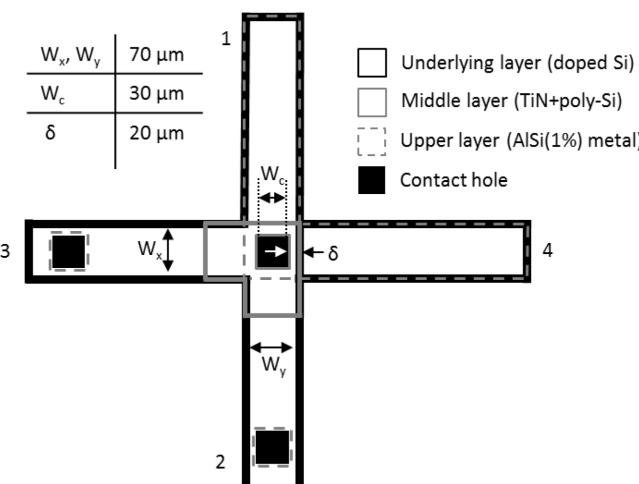


Fig. 4.3 Four terminal CBKR structure with given design parameters.

In addition to resistance measurements, measurement of the gate capacitance is also important for analyzing any additional capacitances, leakage, interface traps, or fixed charges in the gate oxide. For this purpose, capacitors with different areas were designed. Together with dedicated test structures, open and short de-embedding structures were also designed. The designed test structures have a Ground-Signal-Ground (GSG) configuration suitable for RF measurements. Fig. 4.4 shows the planar test structures for C-V measurements as well as its de-embedding pairs. Table 4.3 summarizes the dimensions of the designed test capacitors. As shown in this table, the capacitors include one very wide fin as well as 20-60 parallel narrow fins in the design. The advantage of having parallel fin capacitors is to compare and observe any effect of the edges of the fins.

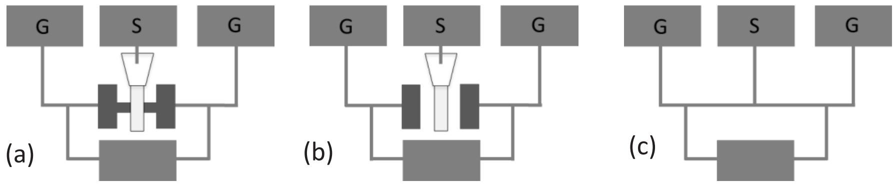


Fig. 4.4 C-V test structures with GSG connections for (a) C-V measurement, (b) open de-embedding and (c) short de-embedding structure.

Table 4.3 *Design parameters of the C-V test structures*

number of fins	W_{FIN} & L_{gate}	W_{FIN} & L_{gate}	W_{FIN} & L_{gate}
1	20 µm & 20 µm	10 µm & 20 µm	4 µm & 20 µm
20	20 nm & 20 µm	30 nm & 20 µm	40 nm & 20 µm
40	20 nm & 20 µm	30 nm & 20 µm	40 nm & 20 µm
60	20 nm & 20 µm	30 nm & 20 µm	40 nm & 20 µm

4.1.2 Processing

As described in section 1.2, (001) oriented SOI wafers are used as a substrate in this work. Initially, the thickness of the Si on oxide was 1.5 µm. By thermally oxidizing Si and wet etching of the oxide, the thickness of the silicon was decreased to 150 nm. The thickness of the Si layer determines the height of the fin. Si fins as well as S/D regions were patterned with an e-beam lithography (EBL) process. Gate patterning was done by photolithography (PL). The alignment of the devices to the crystal orientation is illustrated in Fig. 4.5. The fin sidewall orientation of the devices is $(1\bar{1}0)$ while the surface or crystal plane orientation of the wafer is (001). The crystal orientation of the device is confirmed by TEM analysis in section 4.2.1. To align the EBL patterned features to the PL patterned ones, global alignment crosses as well as write-field alignment crosses were etched through the buried oxide (BOX) layer down to the Si substrate before the device processing. The global alignment crosses are required to find the region of interest for the EBL process. Once the coordinate system is defined, the system is able to find and align the structures to the write-field alignment crosses. Then, the structures can be written with a relatively good alignment. The process flow is depicted in Fig 4.6.

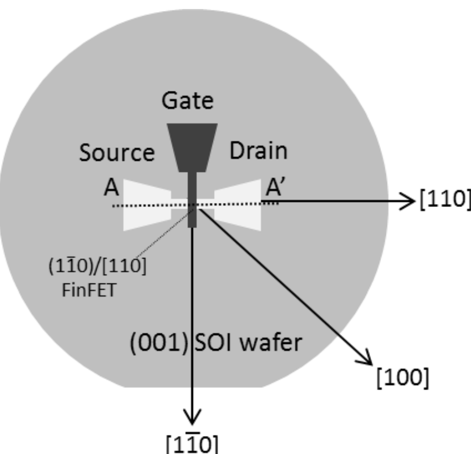


Fig. 4.5 Schematic layout of a $(1\bar{1}0)/[110]$ oriented FinFET fabricated on a (001) SOI wafer. The layout is not to scale. For the sake of clarification the FinFET has been magnified drastically.

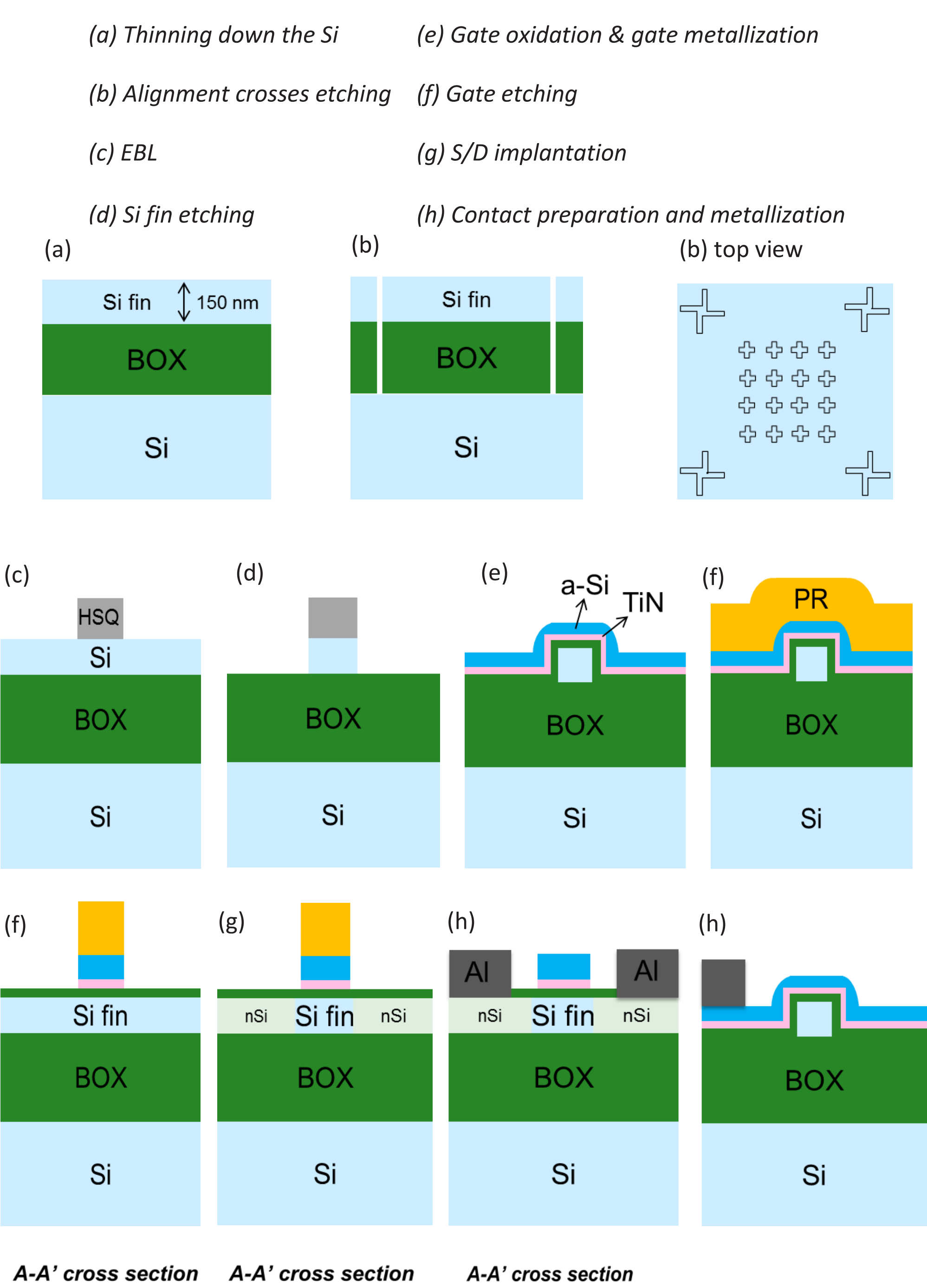


Fig. 4.6 Schematic process flow of the FinFET showing the process steps described in (a)-(h). The A-A' cross sections are taken in the current flow direction as indicated in Fig. 4.5.

The processing can be described in the following order:

(a) Thinning down the Si: The SOI layer thickness was initially 1.5 µm. The Si layer thickness is reduced to 150 nm by a 3 step process. In step 1, the Si was wet oxidized for 6 hours at 1050 °C and then the grown oxide layer of 1050 nm was wet etched in BHF. After this step, the Si layer thickness was measured as 1050 nm with an ellipsometer. In step 2 and 3, the same processing was done as described for step 1. After the 3rd step, the Si layer thickness was reduced to 150 nm. Ellipsometer measurements showed that this Si layer has the right thickness and a good uniformity after etching.

(b) Alignment crosses etching: Alignment crosses are needed for alignment in the e-beam lithography (EBL) and photolithography (PL) process. After patterning with PL using a 1.7 µm thick mask, crosses were etched down to the Si substrate using a 2-step etch process. First, 150 nm Si layer was dry etched in CHF_3+SF_6+O_2 plasma. Next, the BOX layer of 1 µm was wet etched in BHF. Fig. 4.6 (b) shows the side and top view of the crosses for global and manual alignment of the EBL structures.

(c) EBL and (d) Si fin etching: A negative tone HSQ 1541 resist with 4 % concentration was used in the EBL process. After spinning the resist at a rate of 5000 rpm, a 70 nm thick resist layer was obtained on the Si. After the resist processing the EBL exposure was done with 20 keV beam energy, 0.12 nA beam current, 100-300 µC/cm^2 area and 1150-1950 pC/cm line dose, respectively. The EBL process was performed by manually aligning the EBL mask to the alignment crosses etched before. The auto-focus feature of the EBL system was also used to keep the beam focused to the substrate during the complete patterning process. After exposure, the resist was developed in OPD 4262 for 30 sec. The EBL patterned Si fin structures as well as S/D extensions were dry etched in a plasma etcher. RIE was done in Cl_2 (17.5 sccm), HBr (25 sccm) and O_2 (3 sccm) at 10 mTorr with 80 W source power and 350 W RF power. Cl_2 and HBr based recipes are known to have high etch rates for Si and high selectivity to oxide. In this case, we obtained Si:HSQ=10:1 selectivity. Fins and S/D regions were successfully etched in this plasma with a 150 nm/min etch rate and high anisotropy. Subsequently, the HSQ was removed in 30 sec using an HF 1 % solution.

(e) Gate oxidation & gate metallization: After patterning the Si fin and S/D regions, a gate oxide layer of 11 nm was grown by thermal oxidation (measured by ellipsometer). Next, a 6 nm thick TiN layer was deposited with an in-house atomic layer deposition (ALD) system [8] by controlling the growth with an *in-situ* spectroscopic ellipsometer (SE). To prevent the oxidation of TiN when exposed to air, a 12 nm amorphous Si (α-Si) layer was *in-situ* deposited without a vacuum break. The deposition of α-Si was done in the same reactor

at 350 °C by low pressure chemical vapor deposition (LPCVD) at 1 mbar process pressure using trisilane (Si_3H_8) as the source gas.

(f) Gate etching: After the gate layer was patterned by PL using a 1.7 µm thick PR mask, the native oxide was removed in HF solution. And then, the α-Si capping layer etching was first done in a Cl_2 based plasma etcher with a similar process used for the Si fin etching. However, due to the anisotropic nature of the parallel plate plasma etcher, the α-Si layer could not be completely removed from the fin sidewalls. During the subsequent wet etching of the TiN, the α-Si spacer will act as a mask leaving TiN at the sidewall as well. Fig. 4.7 shows a HRSEM picture of the sidewall after α-Si etching. A spacer is clearly observable in this picture. Fig. 4.8 shows the obtained *I-V* curve after finishing the processing of this device. A high gate current of up to 10^{-5} A is observed due to the short circuit between the S/D regions and the gate, formed by a metal spacer. Therefore, an isotropic etching step must be done to remove the materials from the sidewalls of the Si fin. Although less anisotropic etching was achieved by changing the process parameters, we were not able to remove the metal layer completely from the sidewalls using the same plasma etching system.

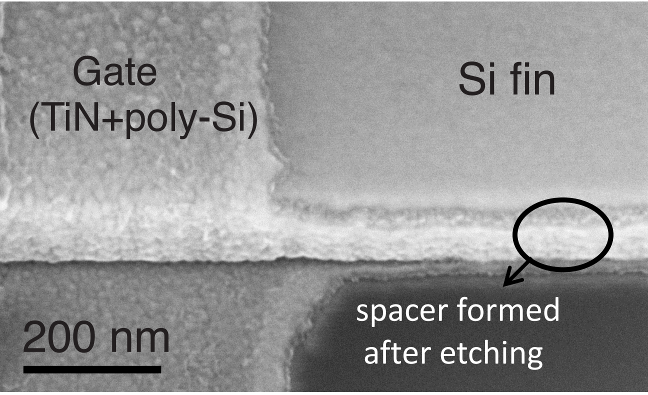


Fig. 4.7 Top view HRSEM picture of the fin sidewall.

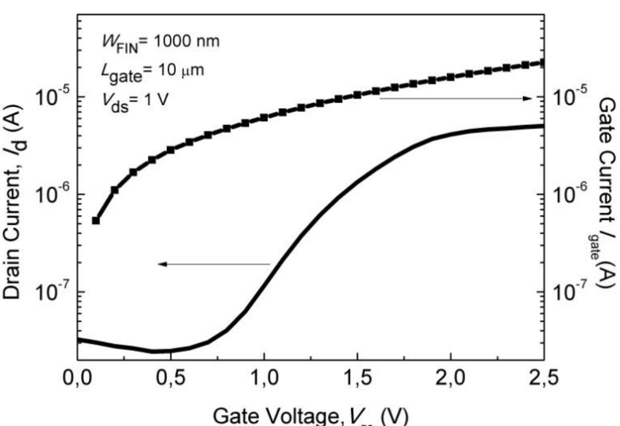


Fig. 4.8 I_d-V_{gs} *and* I_{gate}-V_{gs} device characteristics with W_{FIN}=1000 nm and L_{gate}=10 µm at V_{ds} = 1 V. The obtained high gate leakage current is due to the metal spacers.

In contrast to the parallel plate plasma etching systems, barrel reactors are known to provide isotropic etching. Therefore, the α-Si was dry etched in CF_4/O_2 plasma by using a barrel reactor at the MiPlaza cleanroom, Eindhoven, The Netherlands[1]. High resolution scanning electron microscope (HRSEM) pictures after etching showed that the metallic layer could be completely removed from the sidewalls. After successful etching of the α-Si layer, the TiN layer was wet etched using H_2O_2+NH_4OH+H_2O solution in a 2 min. etching process. Therefore, a much lower gate current was obtained ($\approx 2\text{x}10^{-15}$ A).

(g) S/D implantation: The PR mask used for gate etching was also used for masking the implantation process. The implantation dose parameters were determined by 2D Athena (Silvaco) process simulations. Aiming to have a doping concentration of 10^{19} cm^{-3}, the S/D regions were implanted with As^+ with a 1×10^{15} cm^{-2} dose and at 50 keV. The PR was stripped in O_2 plasma after implantation. After wafer cleaning, a rapid thermal annealing (RTA) was done in a two-step process. Before reaching the maximum temperature, the wafer was maintained at 600 °C for 10 sec and then the RTA at 900 °C for 30 sec was done to activate the dopants. The main reason for this two-step process is to attune the metal stack to a high temperature treatment. Due to high temperature annealing, the α-Si crystallizes. Therefore, it is stated as poly-Si in the rest of this thesis.

It is important to note that the TiN induced strain in FinFETs as discussed in Chapter 2 is not expected in this device structure. First, ALD TiN is known to induce less strain (≈ 50 % less) than physical vapor deposited TiN and it is close to zero for TiN films with a layer thickness below 10 nm [9]. Second, the RTA temperature is 900 °C whereas NXP-TSMC FinFET devices were exposed to 1100 °C. This means that the stress due to the thermal

[1] This part of the processing was performed by R.A.M. Wolters, with courtesy.

expansion coefficient difference between that of the TiN metal gate and the Si will be less. Third, we used an 11 nm thick oxide layer, which is almost 5 times thicker than that of NXP-TSMC FinFETs. This relatively thick oxide layer under the TiN would result in less strain in Si. Therefore, our FinFETs will have a different strain distribution than that of the strained FinFETs discussed in Chapter 2. We expect that the amount of strain is low due to the reasons mentioned above.

(h) Contact preparation and metallization: The metal patterns were defined by PL using a shadow mask. Prior to metal deposition (gate) oxide on the contact holes was removed by 1 % HF etching. Metal deposition was done by sputtering from an Al-Si (1 %) target to obtain a 250 nm thick metal layer. The patterning was finalized by a lift-off process in acetone. As a last step, to reduce the amount of interface traps, 100 % H_2 annealing at 10 mbar was done at 420 °C for 20 min. Fig. 4.9 shows an optical micrograph top view of a fabricated device structure.

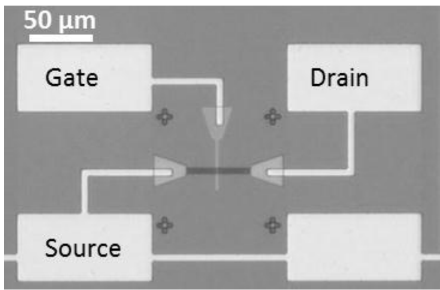


Fig. 4.9 Optical micrograph of a typical FinFET. Note the write field alignment marks are needed for EBL.

4.2 Physical and electrical characterization of FinFETs

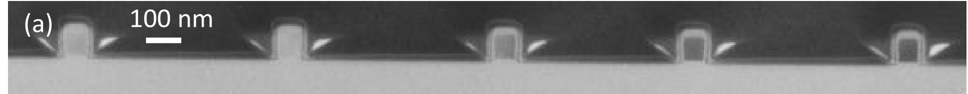
Analyses of the fabricated FinFETs were done by physical and electrical characterization techniques. Focused ion beam (FIB) as well as transmission electron microscope (TEM) were used to study cross sections of the fabricated 3D device structure. The electrical characterization of the FinFETs was done at room temperature by using a SÜSS Microtech probe station equipped with a Keithley 4200 semiconductor characterization system.

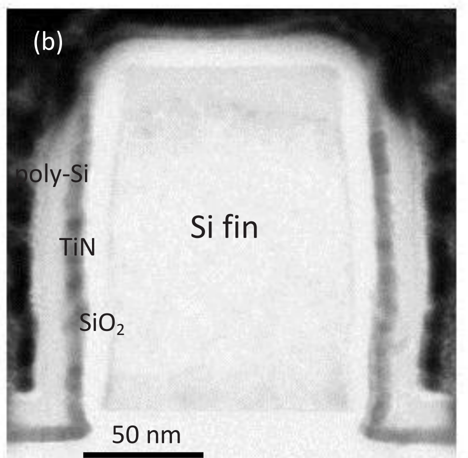
4.2.1 FIB/TEM analysis

To take a cross section picture of the fabricated FinFETs, the sample was prepared with a FIB tool by cutting through the Si fin in the channel region. After preparation, a TEM picture of the FinFET was taken. Fig. 4.10 (a) shows a 5-fin structure with a 100 nm fin width. A closer view of one fin is shown in Fig. 4.10 (b). In addition, a Si fin with 20 nm

designed width is presented in Fig. 4.10 (c). Fig. 4.10 (b) shows that the real fin width is very close to the designed width of 100 nm. Fig. 4.10 (c), on the other hand, shows that the actual fin width is changing along the fin height. The fin width is measured to be ≈ 14 nm for the thickest region. Therefore, the actual fin width is smaller than the designed width of 20 nm. For convenience sake in this work the designed fin width will be used as a reference unless stated otherwise.

The stack of SiO_2+TiN+poly-Si layer is observed around the fin. The cross section picture indicates that the channel is well defined and that the poly-Si/TiN layers have good step coverage. The layers on the sidewalls are clearly observable. The information from the top of the fin was lost due to sample preparation. As will be shown in chapter 5, this region is also clearly observable when there is a PZT layer on top of the fin.





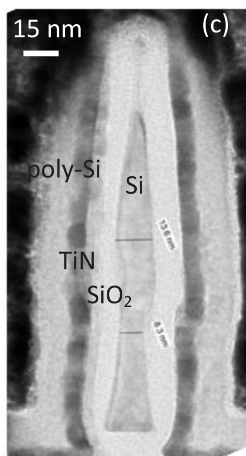


Fig. 4.10 A TEM cross section picture of (a) a 5-fin FinFET with 100 nm fin width, magnified view of a (b) 100 nm and (c) 20 nm wide designed single fin.

4.2.2 Resistance measurements

Resistance measurements give a quick understanding of the basic properties of the thin films. In this section, the GCs presented in Fig. 4.2 and the CBKR presented in Fig. 4.3 are used. These analyses give a quick assessment of the process control. They are important to know before the characterization of the actual FinFETs.

To calculate the doping concentration in the S/D regions and resistivity of the deposited gate stack, sheet resistance measurements were done using the GC I and GC II structures in Fig. 4.2. The sheet resistance of GC I with 1 µm × 1 µm wide arms was determined to be 204 Ω/□. Using this value, the resistivity (ρ) of the doped S/D contact region can be calculated according to [1]:

$$\rho = R_{sh} \times t\ , \tag{4.4}$$

where t is the thickness of the film (*i.e.* 150 nm). The resistivity of the doped Si is calculated being ≈ 3.1 × 10^{-3} Ω-cm using Eq. (4.4). The doping concentration corresponding to this resistivity is around 10^{19} cm^{-3} [10]. This value is in agreement with the projected doping concentration mentioned in section 4.1.2.

The GC I test structure with 100 nm wide arms showed a much higher resistivity than that of 1 µm wide arm. The possible reason for this discrepancy is the incompatibility of the GC method for nanometer sized structures where edge effects become dominant and affects the resistance measurements. Another method can be used to obtain the actual resistivity of such narrow structures, such as the transfer length method [1]. The sheet resistance obtained from the GC II with 5 µm × 5 µm and with 10 µm × 10 µm wide arms is 264 Ω/□. Using Eq. (4.4), the resistivity of the TiN is calculated to be ≈ 160 µΩ-cm. This value is in agreement with the value obtained from the different structures using the same setup [11]. The sheet resistance of the GC III was measured as ≈ 3×10^{5} Ω/□. This high value is an indication that there are no active dopants in the Si channel, as expected from TCAD simulations.

To obtain the specific contact resistance, the CBKR structure shown in Fig. 4.3 was measured. The resistance is measured as R_k= 35 Ω by applying a current between pad 1 and 3 and measuring voltage in pad 3 and 4. ρ_c can be calculated using Eq. (4.3) and inserting the known parameters. The calculated ρ_c is in the order of 10^{-4} Ω-cm^2. This value is in the same order of magnitude as mentioned in previous reports [12].

4.2.3 *I-V* characterization and analysis

FinFETs with different W_{FIN} and L_{gate} were measured and analyzed. Most of the single fin devices, especially with narrow fins, were not functional. 5-fin devices, on the other hand, showed better characteristics. All presented characteristics belong to devices with 5-fins unless stated otherwise. Fig. 4.11 shows the I_d-V_{ds} curve of the eight different fabricated FinFETs.

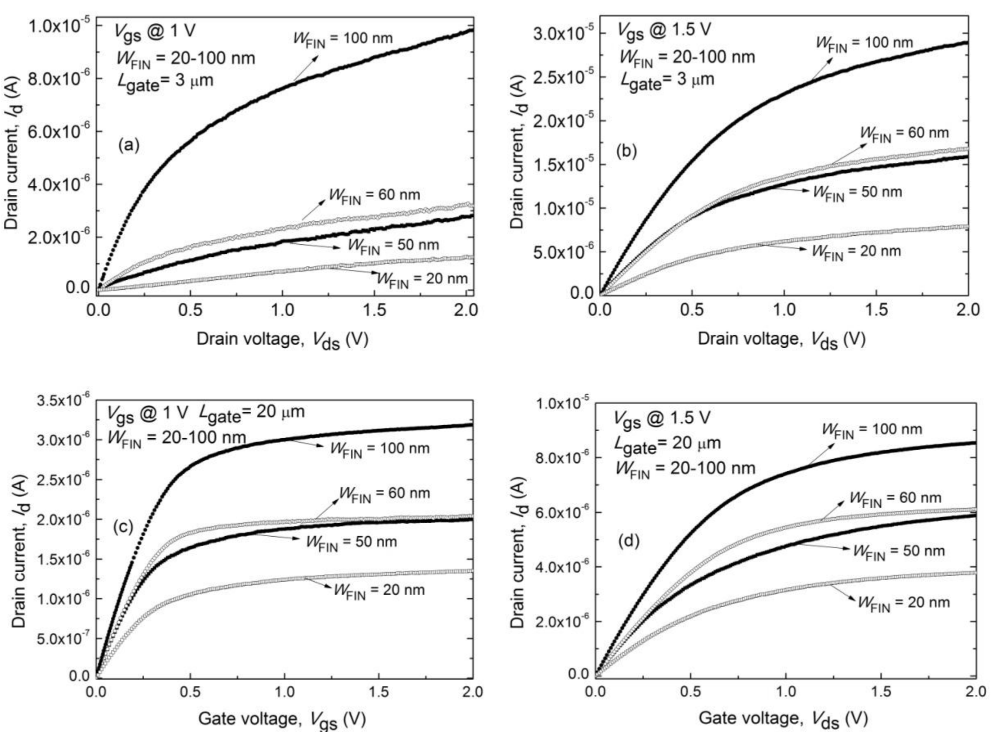


Fig. 4.11 I_d-V_{ds}characteristics of devices with W_{FIN}= 20 nm-100 nm and (a) L_{gate}= 3 μm, V_{gs}= 1 V, (b) L_{gate}= 3 μm, V_{gs}= 1.5 V, (c) L_{gate}= 20 μm, V_{gs}= 1 V, (d) L_{gate}= 20 μm, V_{gs}= 1.5 V. The measurements were performed at 300 K.

In typical I_d-V_{ds} curves, there are three regimes of operation, namely linear, non-linear and saturation regions [10, 13]. In the linear region, where V_{ds} is less than V_{gs}, the drain current of long channel FETs can be expressed as follows:

$$I_d = \mu_n C_{ox} \frac{W}{L_{gate}} [(V_{gs} - V_{th})V_{ds} - \frac{1}{2} V_{ds}{}^2] , \quad (4.5a)$$

whereas in the saturation region the drain current can be expressed as [13]:

$$I_d = \mu_n C_{ox} \frac{W}{L_{gate}} (V_{gs} - V_{th})^2 , \quad (4.5b)$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W is the channel width (= N_{FIN} x (2 H_{FIN} + W_{FIN}), N_{FIN} is the number of active fins), L_{gate} is the gate length, V_{th} is the threshold voltage; the gate-source voltage at which the inversion layer is formed at the interface between the gate oxide and the Si.

Fig. 4.11 shows the I_d-V_{ds} curves for short channel (3 µm gate length) and long channel devices (20 µm gate length). The latter was chosen to reduce short channel effects and to avoid a high S/D resistance. It can be concluded from the figure that the I_d does not scale with the channel width as described by Eq. (4.5b). In fact, I_d generally increases more sharply with *W* and this could be due to several effects.

First, if the fin width decreases, the resistance of the S/D extensions will become dominant, especially for the short gate length. This results in a decrease in the drain current, especially in the linear region above threshold. This phenomenon can be observed when Fig. 4.11 (a) and (c) are compared for narrow fins. In addition, irregular fin width results a smaller average fin width over the fin height (Fig. 4.10), which causes nonlinearity. The drain current scaling is more non-ideal for devices with 3 µm gate lengths compared to devices with 20 µm gate lengths.

Second, a change in the effective channel length can result in stronger than expected scaling of I_d. Since the doping in the channel region is very low (≈ 10^{15}cm^{-3}), as confirmed in our GC III structures, the depletion layer laterally extends further in the channel region for a wide fin than for a narrow fin device because of improved electrostatic gate control for the latter. This is observed in the saturation region in which the "Early effect" [10] seems to be stronger for a wide fin (Fig. 4.11 (a) and (b)). However, when the channel length is longer, this effect is less important (Fig. 4.11 (c) and (d)).

Third, one or more defective fins and/or line edge roughness (LER) could be the reason for this strong dependency. The LER effect has been shown to be the main source of variability in FinFET devices [14, 15].

Fourth, non-uniform doping in the S/D extensions regions can result in high I_{on} variability. This effect is more serious for narrow fins and short gate lengths [16]. It could be an indication of less strong scaling observed in our long channel devices in Fig. 4.11 (c) and (d).

The FinFET is in a weak-inversion or depletion mode in the sub-threshold region and the drain current is dominated by diffusion. This region of operation is important to study since this region characterizes how sharply the current drops with the gate bias. This region is important for low power applications. The drain current of a long channel fully depleted FinFET operated at gate voltages below threshold is [13]:

$$I_d = \frac{N_{FIN} H_{FIN} \mu_n}{L_{gate} \beta} q\, n_i W_{FIN} \exp(\beta \varphi_s) [1 - \exp(-\beta V_{ds})] \ , \qquad (4.6)$$

where β=q/kT, μ_n is electron mobility, n_i is intrinsic carrier concentration, and φ_s is the surface potential.

For a fully depleted FinFET the following relation can be obtained:

$$V_{gs} - V_{fb} = \frac{Q_{it}}{C_{ox}} + \varphi_s = \left(\frac{C_{it}+C_{ox}}{C_{ox}}\right) \cdot \varphi_s \quad , \tag{4.7}$$

where Q_{it} is the interfacial trapped charge and V_{fb} is the work function difference between intrinsic silicon and the gate metal (V_{fb}=0 V for a mid-gap metal gate).

The relative change of V_{gs} caused by φ_s can be found using Eq. (4.7):

$$\frac{dV_{gs}}{d\varphi_s} = \frac{C_{ox}+C_{it}}{C_{ox}} \equiv \mathrm{n} \, . \tag{4.8}$$

Using Eq. (4.8), Eq. (4.6) can be rewritten as

$$I_d = I_{d1} \exp\big(\beta\big(V_{gs} - V_{fb}\big)/\mathrm{n}\big) \left[1 - \exp(-\beta V_{ds})\right] , \tag{4.9}$$

where I_{d1} depends on temperature, device dimensions and n is the ideality factor. In an ideal FinFET with a negligible amount of interfacial traps, n=1.

For $V_{ds} >> kT/q$, Eq. (4.9) can be simplified as:

$$I_d = I_{d1} \exp\big(\beta\big(V_{gs} - V_{fb}\big)/\mathrm{n}\big) \, . \tag{4.10}$$

Hence, the sub-threshold current in which log (I_d) is plotted vs. V_{gs}, has a slope of $q/[\ln(10) \cdot \mathrm{n}kT]$. The so-called sub-threshold swing (*SS*) is defined as the inverse of that value, $\ln(10) \cdot \mathrm{n}kT/q$ [10], corresponding to approximately 60 mV/dec at room temperature for an ideal FinFET (without any traps).

In Fig. 4.12, experimental I_d-V_{gs} curves of FinFETs with a different W_{FIN} are shown for V_{ds}= 25 mV (a) and V_{ds}= 1 V (b). These curves show a high on- to off-current ratio I_{on}/I_{off} ($\approx 10^8$) and a *SS* value of 76 mV/dec.

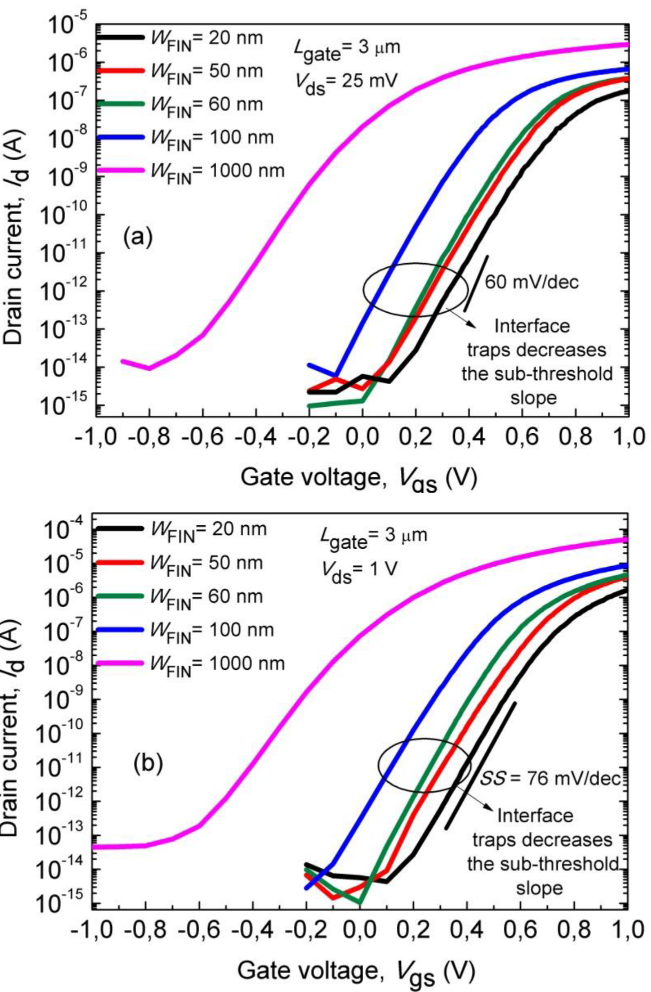


Fig. 4.12 I_d-V_{gs} characteristics of devices with L_{gate}= 3 µm and W_{FIN}= 20 nm-100 nm, at (a) V_{ds}= 25 mV and (b) V_{ds}= 1V.

As discussed before, the drain current I_d increases stronger than expected with the channel width (*W*). In addition, we observe a short-channel effect for W_{FIN}=1000 nm, which is due to less electrostatic gate control, resulting in an increased *SS*. This effect is related to the so-called drain-induced barrier lowering, or in short DIBL [10], as discussed later.

Another important observation is an increase of the threshold voltage when the fin width decreases. The proportionality of the sub-threshold current to the Si thickness is a manifestation of volume inversion [13]. In the ultra-thin body, there is a limited amount of inversion charge [17] and this is observed as a decrease in the sub-threshold current.

To compare the performance, I_d-V_{gs} characteristics of NXP and our FinFET devices measured at V_{ds}= 1 V are plotted in Fig. 4.13.

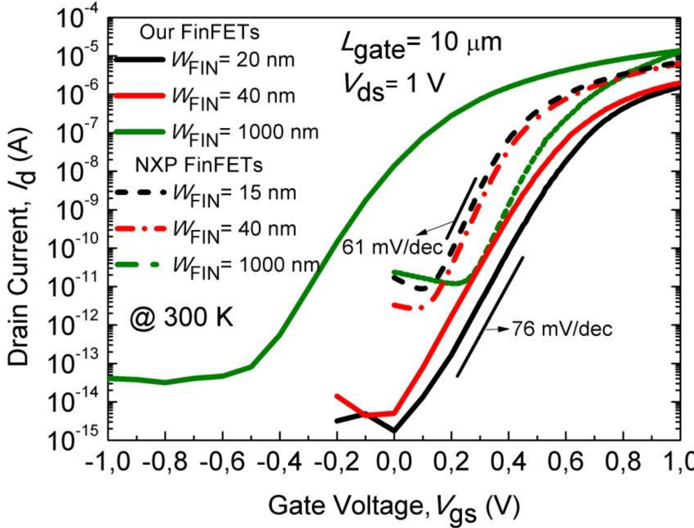


Fig. 4.13 I_d-V_{gs} characteristics of NXP and our FinFET devices with 5-fins, L_{gate}= 10 µm and W_{FIN}= 20 nm, 40 nm and 1000 nm at V_{ds}= 1V. The measurements were performed at 300 K.

Due to shorter S/D extensions in NXP FinFETs (L_{sd}=90 nm) compared to our FinFETs (L_{sd}=15-23 µm), I_{on} is around three times higher for NXP FinFETs for narrow fin devices. Furthermore, I_{off} is higher and *SS* is lower for NXP FinFETs (≈ 10^{-11} A and ≈ 61 mV/dec) than UT FinFETs (≈ 10^{-14} A and ≈ 76 mV/dec). The lower *SS* is due to less interface states. To summarize, our devices perform well as evidenced by this comparison.

The amount of active interface states in our devices can be calculated using the *SS* value. The amount of increase in Q_{it} would increase the n value in Eq. (4.8). The value n can be obtained for UT FinFETs by dividing the *SS* to the ideal *SS*, n=1.27. Therefore, C_{it}/C_{ox}=0.27. As will be shown later in section 4.2.4, C_{ox}=3.1x10^{-7} F/cm^2. Therefore, C_{it} = 8.37x10^{-8}F/cm^2. Since for the interface trap density holds D_{it}=C_{it}/q^2 [1], D_{it} can be calculated as 5.23x10^{11} 1/eV-cm^2.

Drain-induced-barrier lowering (DIBL) is another performance degrading mechanism resulting in a shift of the threshold voltage at high drain voltages and consequently high I_{off}. This effect strongly depends on the channel length. In principle a higher body doping and/or an improved gate control through a narrow fin width is required to reduce this effect by preventing the expansion of drain depletion into the channel. However, high doping results in lower mobility, higher junction capacitance and increased junction leakage [18]. For our FinFETs, the DIBL is shown in I_d-V_{gs} curve at different V_{ds} in Fig.

4.14. DIBL is defined as the decrease in threshold voltage when the drain voltage is increased from 25 mV to 2 V. DIBL is calculated as 93 mV/V, using the following relation:

$$\text{DIBL (mV/V)} = \frac{V_{th1} - V_{th2}}{V_{ds1} - V_{ds2}}. \quad (4.11)$$

Although our devices have a low channel doping, they do not suffer from strong DIBL. This is because our device lengths are in the micrometer range and we use narrow fins. The calculated DIBL value is comparable to the values obtained from simulations by Lee *et al.* using similar device structures [19].

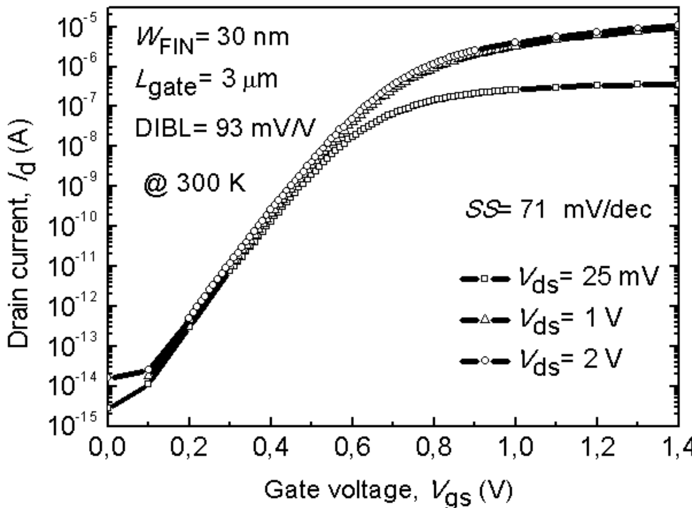


Fig. 4.14 I_d-V_{gs} curves of devices with L_{gate}= 3 µm and W_{FIN}= 30 nm, at V_{ds}= 25 mV, 1 V and 2 V. The measurements were performed at 300 K.

As mentioned before, an increase in the channel length decreases the sub-threshold leakage by suppressing the short channel effects (SCE). However, it also increases the channel resistance, thereby decreasing I_{on}. I_{on} and I_{off} gets smaller for longer gate lengths because of lower leakage and higher channel resistance.

Fig. 4.15 shows I_d-V_{gs} curves obtained from devices with various fin widths and gate lengths at V_{ds}= 1 V. The I_{off} and I_{on} scaling with gate length stated before is only observed in Fig. 4.15 (d) for the W_{FIN}= 1 µm device. Figs. 4.15 (a)-(c) show that I_{off} and I_{on} show no clear dependency on the gate length for narrow fins. As mentioned in section 4.2.3, the cause of this scaling deficiency is possibly caused by defective fins, LER, S/D doping non-uniformity. Furthermore, positive fixed charges at the interface (or in the gate oxide) and interface states (traps) could give a channel length dependence of this effect. Stronger than expected gate length scaling of the drain current holds especially for devices having a narrow fin width and long gate length. This dependence could be due to

the etching process. While etching the fins, surface imperfections could have been created, which would be more important for narrow fins and long gate lengths. The TEM picture especially for the 20 nm specified fin width in Fig. 4.10 clearly shows that the actual fin width is smaller than the specified width and also varies over the fin height. The latter also reduces drastically in particular on top of the fin. This could cause an increase of the threshold voltage or the actual average W_{FIN} drops drastically. As a result, the sub-threshold current drops (see Eq. (4.6)). This irregular fin sidewall pattern could also vary across the gate length. Further, other non-idealities such as fixed charge or additional traps could also have been formed by the etching process. Since both sub-threshold and up-threshold region are affected, more than one of these non-idealities could be present.

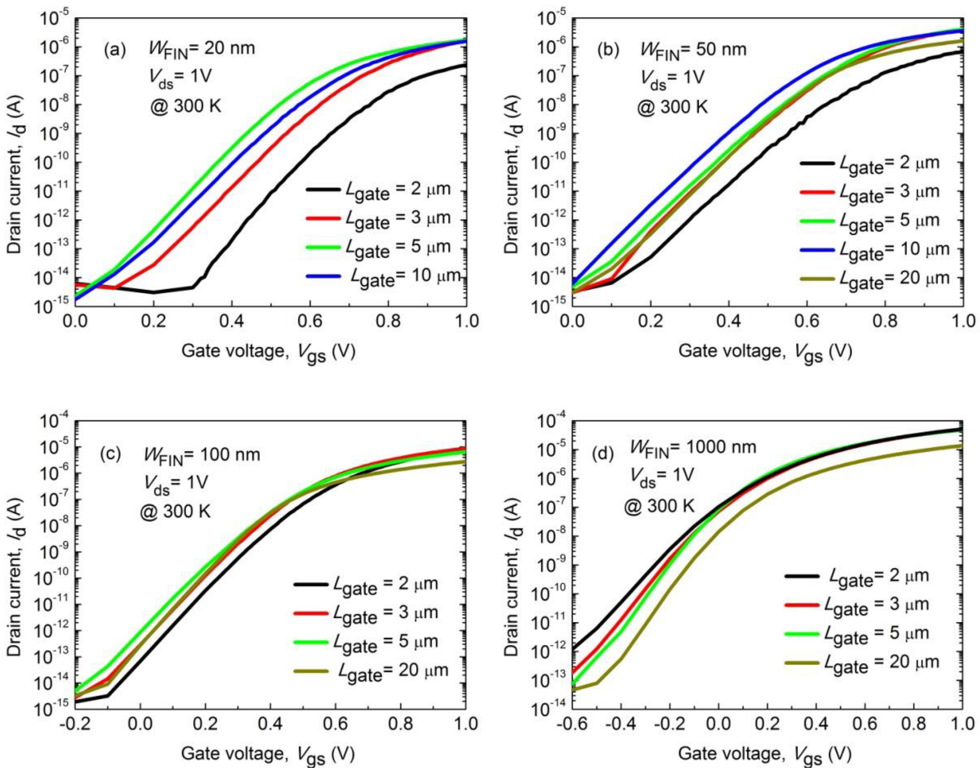


Fig. 4.15 I_d-V_{gs} device characteristics with L_{gate}= 2-20 µm at V_{ds}= 1 V for a) W_{FIN}= 20 nm, b) W_{FIN}= 50 nm, c) W_{FIN}= 100 nm, and d) W_{FIN}= 1000 nm. The measurements were performed at 300 K.

4.2.4 Mobility calculation

Mobility extraction of the FinFET is not very straightforward due to some complications such as the body doping effect and different turn on voltages at the top corners and the body of the fin. In this work, the body doping is negligible (≈ 10^{15} cm^{-3}) and hence the structure does not suffer from different turn on voltages. As a result, there is no "kink" in the presented sub-threshold curves.

The mobility of the measured (long channel) FinFETs can be calculated using the following drift and diffusion current relation:

$$I_d = \frac{W \mu_{eff} Q_n V_{ds}}{L_{gate}} - \frac{N_{FIN} H_{FIN} \mu_{eff} kT}{q} \frac{dQ_n}{dx}, \quad (4.12)$$

where Q_n is the mobile charge density (C/cm^2), μ_{eff} is the effective mobility generally measured at low V_{ds} (hence low lateral electric field). At low V_{ds} (25-100 mV) and above threshold voltage, the carriers in a uniformly doped channel are uniformly distributed. Therefore, the diffusive second term in Eq. (4.12) can be ignored. To obtain an μ_{eff} expression, the mobile charge density needs to be determined. One way to do so is to approximate it by:

$$Q_n = C_{ox}(V_{gs} - V_{th}). \quad (4.13)$$

Although it is an easy way to determine Q_n, the charge density is not exactly given by this expression. However, it is a good approach to obtain the mobility for above threshold and would give representative numbers.

Inserting Eq. (4.13) in Eq. (4.12) and ignoring the diffusive second term, μ_{eff} can be expressed as:

$$\mu_{eff} = \frac{I_d L_{gate}}{W C_{ox}(V_{gs} - V_{th}) V_{ds}}. \quad (4.14)$$

C_{ox} is the oxide capacitance per unit area (specific oxide capacitance) and can be calculated using the following relation:

$$C_{ox} = \frac{C_{ox}'}{A} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}, \quad (4.15)$$

where $\varepsilon_0 \varepsilon_{ox}$=3.45×$10^{-11}$ F/m, and t_{ox}=11 nm, A= N_{FIN} × [{(2 × H_{FIN}) + W_{FIN}} × L_{gate}]. Therefore, the oxide capacitance per unit area for these devices was calculated as 3.1×10^{-7} F/cm^2. This value is in good agreement with the measured capacitance values as shown in section 4.2.5.

The I_d-V_{gs} curves (at V_{ds} = 25 mV) plotted in Fig. 4.16 are used for mobility calculations in Fig. 4.17. Before starting to analyze the mobility graphs, it is wise to first have a look at the behavior of the I_d-V_{gs} curves in linear scale. For an ideal device, a linear relationship between drain current and gate voltage is expected; otherwise Eq. (4.12) cannot be used. Fig. 4.16 shows that the curves deviate from linear behavior for 20 nm and 50 nm wide devices. The deviation starts at about 0.8 V. The reason for this non-linearity is the S/D resistance, adding as a series resistance to channel resistance and becoming more profound for narrow channels and short gate lengths [20]. This effect is important and has to be taken into account while analyzing the mobility graphs.

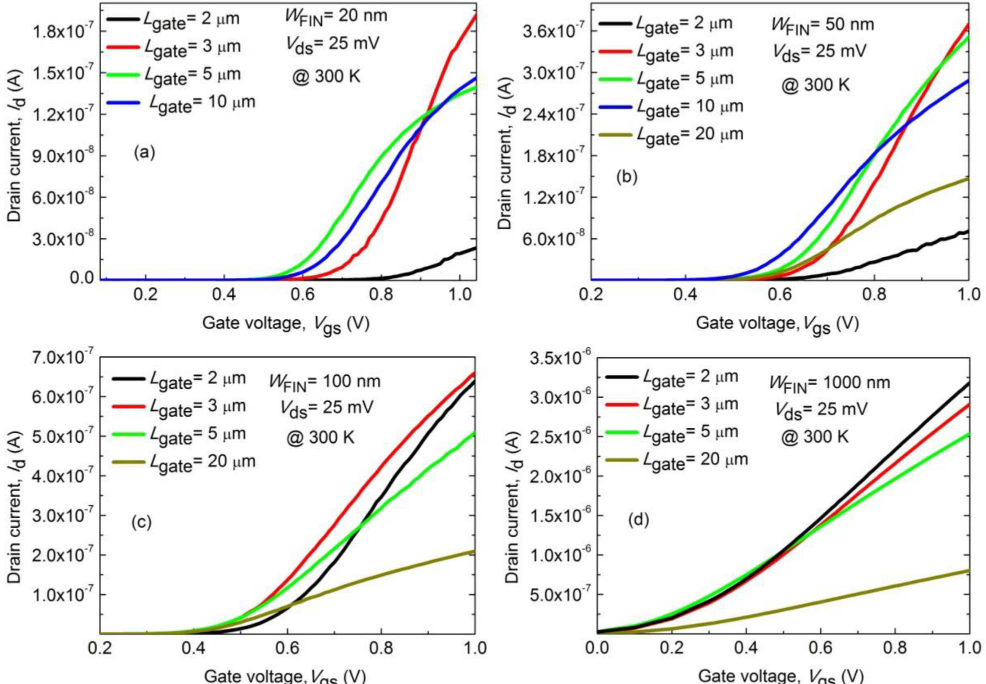


Fig. 4.16 I_d - V_{gs} device characteristics for L_{gate}= 2-20 µm at V_{ds} = 25 mV for 5-fin devices with a) W_{FIN}= 20 nm, b) W_{FIN}= 50 nm, c) W_{FIN}= 100 nm, and d) W_{FIN}= 1000 nm. The measurements were performed at 300 K.

The effective mobility is plotted against the surface electric field of Si. Since an ensemble of electrons that is averaged over the inversion layer, the measured mobility is often called "effective" mobility. Since our FinFETs are fully depleted the surface electric field of Si perpendicular to the current flow direction is given by:

$$E = \frac{Q_{inv}}{\varepsilon_{Si}} \approx \frac{C_{ox}(V_{gs} - V_{th})}{\varepsilon_{Si}}, \qquad (4.16)$$

where Q_{inv} is the inversion charge per unit area. Note that Eq. (4.16) does not represent the effective field [21], rather the maximum field in the Si. By using the Eq. (4.14) and Eq. (4.16), μ_{eff} and E can be calculated. The μ_{eff}–E curves for different fin widths and gate lengths are plotted in Fig. 4.17.

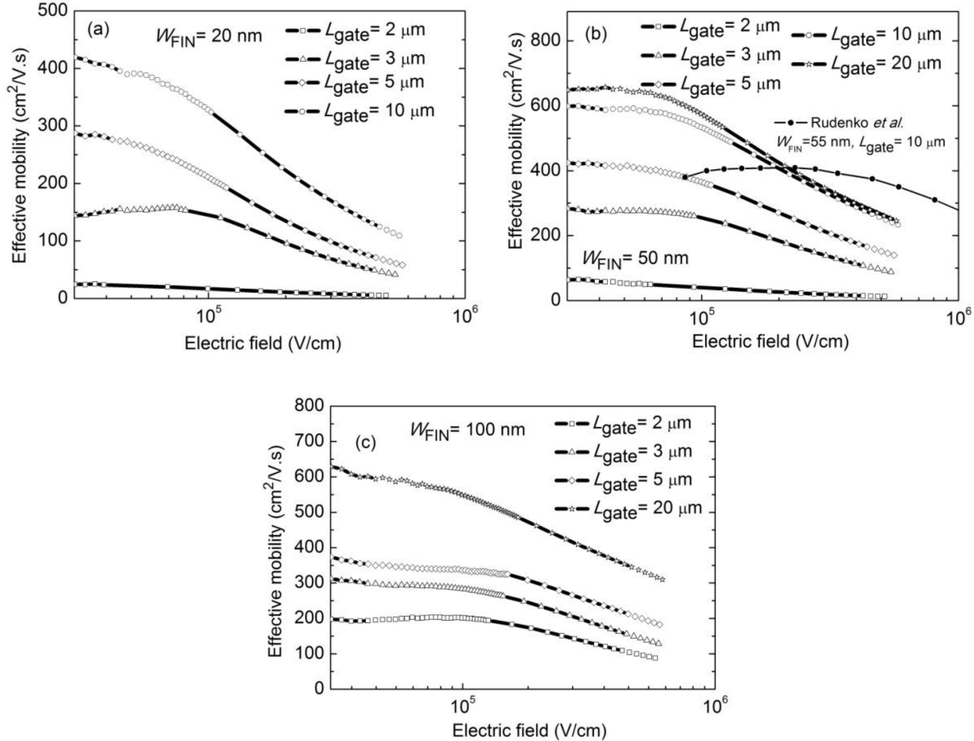


Fig. 4.17 Effective mobility-electric field curves of 5-fin devices with (a) W_{FIN}=20 nm, (b) W_{FIN}=50 nm and (110) n-FinFET with W_{FIN}=55 nm obtained from Rudenko *et al*. [22], (c) W_{FIN}=100 nm and L_{gate}=2-10 μm.

Figs. 4.17 (a)-(c) show that effective mobility is depending on the W_{FIN} and L_{gate}. Short channel effects make the calculations less accurate, especially for wide fins. Therefore, the effective mobility-electric field curve is not shown for a 1000 nm wide device.

In Fig. 4.17 (b), when W_{FIN}=50 nm, the highest effective mobility is obtained. An increase in effective mobility for a narrow fin device was expected since the carriers are being transported through the body (i.e. volume inversion), encountering less surface scattering. However, if the fin width decreases below 10 nm, the body size becomes so small that the electron transport also occurs at the surfaces, resulting in a lower mobility [23, 24]. Although the volume is still large enough for the specified W_{FIN}=20 nm to neglect this effect, it is shown in Fig. 4.17 (a) that the mobility for this device is lower than the device with W_{FIN}= 50 nm. This can be attributed by the smaller and irregularly distributed

actual fin width over the fin height as shown in our TEM analysis (Fig. 4.10 (c)) and possibly due to the series resistance effect, as mentioned before in section 4.2.3. For comparison, effective mobility-electric field curve presented by Rudenko et al. [22] is also drawn in Fig. 4.17 (b). Although the effective mobility values are comparable to the calculated values in this work, the field dependence of the mobility is different. The discrepancy at high fields could be due to an increased surface scattering caused by the irregular fin pattern for our devices.

Especially for 20 nm and 50 nm wide devices, the mobility for the 2 µm gate length is very low, since the effect of the S/D resistance is more profound for narrow channel devices with short gate lengths (see Fig. 4.17 (a)). The mobility shows a dependence on the gate length also. As can be seen in Figs. 4.17 (a)-(c), devices with a longer gate length have a higher mobility for all fin widths. As mentioned before, the S/D extension resistances add as a series resistance to the channel resistance at high fields (in this case above $\approx 6 \times 10^4$ V/cm). However, below this field the effect of the S/D resistance is not important. Another possible reason for mobility degradation could be negative fixed or mobile charges at the gate edges close to the S/D regions [25]. This is highly possible for our devices since an increase in the threshold voltage is observed for shorter gate lengths.

4.2.5 *C-V* characterization

Dedicated *C-V* test structures with GSG connections together with their open and short de-embedding pairs were designed for different dimensions. Each capacitance measurement was performed by de-embedding the pad as well as the parasitic connections. The capacitor dimensions are summarized in Table 4.3, section 4.1.1. The measurements were performed at V_{ac}= 20 mV and at 1 MHz frequency.

Fig. 4.18 shows the *C-V* curves obtained from planar capacitors for W_{FIN}=4 µm, 10 µm, 20 µm and L_{gate}= 20 µm. The specific oxide capacitance was calculated using Eq. (4.15) by changing the value of the capacitor area. The calculated and measured capacitance values at strong inversion are presented in Table 4.4.

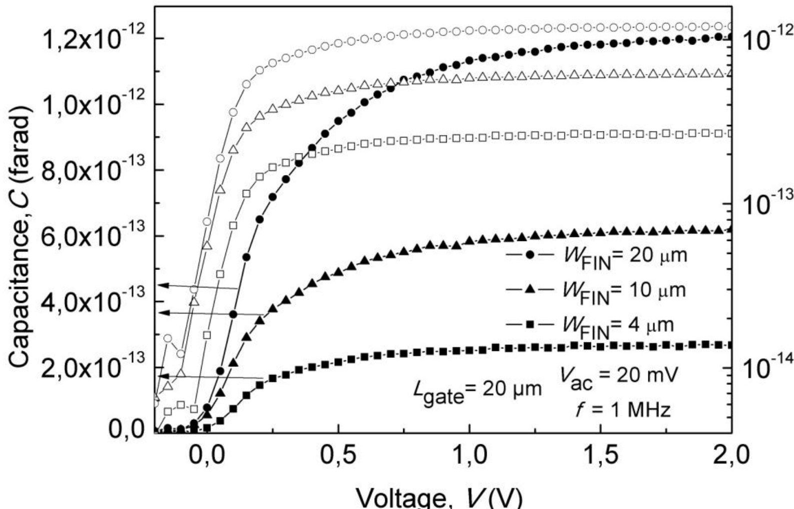


Fig. 4.18 *C-V* characteristics of capacitance test structures for W_{FIN}= 4 µm, 10 µm, 20 µm and L_{gate}= 20 µm. Graphs are plotted in linear and logarithmic scale. Measurements were performed at f = 1 MHz with V_{ac}= 20 mV.

Table 4.4 *Calculated and measured (strong inversion) capacitance values for planar C-V test structures*

	Calculated Capacitance	***Measured Capacitance***
$\boldsymbol{W_{FIN}}$**=4 µm,** $\boldsymbol{L_{gate}}$**= 20 µm**	2.5×10^{-13} F	2.7×10^{-13} F
$\boldsymbol{W_{FIN}}$**=10 µm,** $\boldsymbol{L_{gate}}$**= 20 µm**	5.9×10^{-13} F	6.1×10^{-13} F
$\boldsymbol{W_{FIN}}$**=20 µm,** $\boldsymbol{L_{gate}}$**= 20 µm**	1.2×10^{-12} F	1.2×10^{-12} F

The calculated and measured capacitance values for each capacitor are almost equal. Hence, the measured capacitance at strong inversion mainly includes the oxide capacitance. The amount of interface traps associated to the sub-threshold slope was calculated in section 4.2.4.

The same measurements were performed using parallel fins with narrow fin widths. The dimensions of these test structures are given in Table 4.5. The measurements on parallel fin capacitors were also performed at f=1 MHz, with V_{ac}= 20mV and the results are shown in Fig. 4.19. In this figure, the capacitance values for 20, 40 and 60 parallel fins with W_{FIN}= 20 nm, 30 nm, 40 µm and L_{gate}= 20 µm are plotted. The calculated and measured capacitance values at strong inversion are given in Table 4.5.

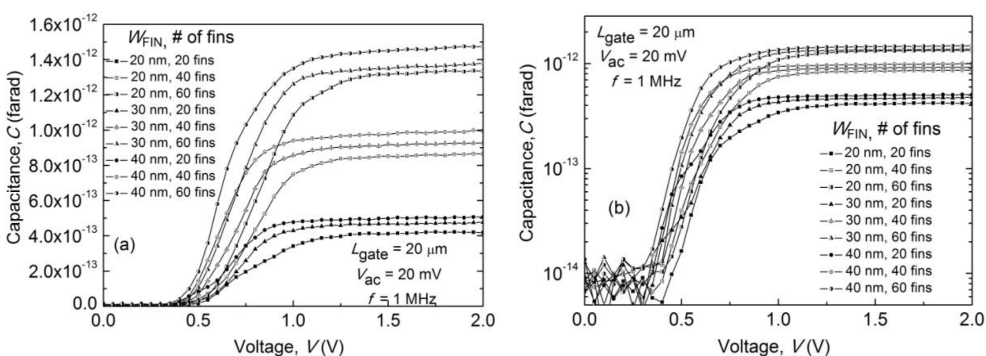


Fig. 4.19 *C-V* characteristics of capacitor test structures for different areas, scaling with W_{FIN} and number of fins in (a) linear and (b) logarithmic scale. Measurements were performed at f = 1 MHz with V_{ac}= 20 mV.

Table 4.5 *(a) Calculated and (b) measured capacitance values for parallel fin C-V test structures*

(a) Calculated	***Capacitance for 20 fins***	***Capacitance for 40 fins***	***Capacitance for 60 fins***
W_{FIN}=20 nm, L_{gate}= 20 μm	4.0×10^{-13} F	8.0×10^{-13} F	1.2×10^{-12} F
W_{FIN}=40 nm, L_{gate}= 20 μm	4.3×10^{-13} F	8.5×10^{-13} F	1.3×10^{-12} F
W_{FIN}=60 nm, L_{gate}= 20 μm	4.5×10^{-13} F	9.0×10^{-13} F	1.4×10^{-12} F
(b) Measured	***Capacitance for 20 fins***	***Capacitance for 40 fins***	***Capacitance for 60 fins***
W_{FIN}=20 nm, L_{gate}= 20 μm	4.1×10^{-13} F	8.6×10^{-13} F	1.3×10^{-12} F
W_{FIN}=40 nm, L_{gate}= 20 μm	4.7×10^{-13} F	9.3×10^{-13} F	1.4×10^{-12} F
W_{FIN}=60 nm, L_{gate}= 20 μm	5.0×10^{-13} F	9.9×10^{-13} F	1.5×10^{-12} F

The calculated capacitance values are in agreement with the measured (strong inversion) values shown in Fig. 4.19. No significant difference is observed in the slope, which points out that the trap density has not changed much. The difference observed between Fig. 4.18 and Fig. 4.19 is the threshold voltage shift of about 0.4 V. The shift *C-V* curves can be attributed to irregular fin pattern (see Fig. 4.10 (c)) and higher amount of surface charge. Both these non-idealities are related to the processing. Each fin has two sidewalls which were formed in the dry etching process. This type of etching process results in surface imperfections. Compared to planar capacitors, parallel narrow fin capacitors are more

eligible for surface imperfections and interface charges, which explain the shift in Fig. 4.19. In addition, as explained in section 4.2.3, narrow fin devices have a limited amount of inversion charge, which results in a decrease of the sub-threshold current and hence, a positive shift.

4.3 Conclusions

In this chapter, the fabrication and characterization of FinFETs are presented. As a first step in the processing, the (001) surface orientated SOI layer was thinned down to 150 nm. After patterning the Si fins with EBL, a gate oxide layer was thermally grown and a TiN+α-Si deposition was done. After patterning the gate metal, ion implantation and RTA were performed. As a final step, contact pads were defined by Al-Si (1 %) sputtering through a shadow mask.

Physical and electrical characterization of the fabricated structures has been discussed showing that devices have a Si body of down to 14 nm width and an aspect ratio of up to 7.5. The TEM analysis also shows that the FinFETs comprise a well defined surrounding gate stack. Resistivity measurements on dedicated process control test structures show that the sheet resistances of the S/D regions as well as gate stack are well in line with TCAD simulations.

The fabricated devices were further analyzed by *I-V* and *C-V* measurements. Electrical measurements revealed that 3 out of 5 devices function well. *SS* of I_d-V_{gs} curves for the devices with W_{FIN}= 20-100 nm and L_{gate}= 3 µm is determined to be 76 mV/dec. A low leakage and high I_{on}/I_{off} (≈ 10^8) together with a DIBL of 93 mV/V are obtained. These values as well as the comparison with the NXP-FinFETs indicate that the fabricated FinFETs have a satisfactory performance.

The gate length scaling of the drain current is discussed and shown for above-threshold region. The results indicate that, for devices with narrow fins and short gate lengths, the S/D resistance becomes more profound. In addition, higher threshold voltages are obtained which can be attributed to the irregular fin width pattern directly or indirectly leading to fixed charge or traps at the gate edges near the S/D regions. These charges are more effective for short channel gates. As a result, a decrease in drain current is observed. However, for devices with wide fins, the current is affected by short channel effects because of the combination of a lowly doped silicon body and poor electrostatic gate control. The effective mobility-electric field curve for long gate lengths (≈ 10 µm) show comparable values as reported in the literature.

C-V analysis has been performed on dedicated test capacitors. Good agreement has been obtained with calculated and measured oxide capacitance values, for both planar and

narrow fin capacitors. A threshold voltage shift is observed for narrow fin structures. This effect is due to narrow channel's limited amount of carriers, which is more profound due to irregular fin width over the fin height, and higher negative charges at the fin sidewalls due to the dry etching process.

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5 The PiezoFET: a piezoelectric layer around a FinFET

In this chapter, the integration and use of a piezoelectric layer as a channel stressor is discussed. A novel four terminal (4T) device structure, called the PiezoFET, will be introduced. The process integration steps and device characteristics of this device are presented. No harmful effects have been observed in device properties after deposition of the piezoelectric material PZT. A high piezoelectric response in the range of 100 pm/V has been obtained for the PZT PiezoFET evidencing the converse piezoelectric effect in the 4T device. As expected, for the AlN PiezoFET the response was less (13 pm/V). Furthermore, a 20-50 % change in the electron mobility and a drastic change in the subthreshold swing (up to 20%) has been observed. The major effect on both mobility and subthreshold swing can be attributed to the strain formed by the difference in thermal expansion coefficient of Si and the PZT layer. It is also partly affected by the bias over the piezoelectric layer, which indicates converse piezoelectric effect related strain in both the silicon channel and gate oxide.

5.1 The piezoelectric layer as a stressor

As discussed in chapter 3, ferroelectric materials are of high interest for device applications. In this chapter, we are interested in the *converse* piezoelectric effect of a commonly used ferroelectric material, called lead-zirconate-titanate ($Pb[Zr_xTi_{1-x}]O_3$) or in short PZT. PZT was chosen because of its high piezoelectric response among other piezoelectric materials [1]. It has been recently reported that the piezoelectric properties can be utilized for a strained silicon (Si) device application [2].

The converse piezoelectric coefficient of a material relates the mechanical displacement to the applied electric field [3]. The deformation can be along or perpendicular to the applied field, i.e. the longitudinal or transverse piezoelectric effect. The strain at the channel of a FET changes the electrical device characteristics. Using the reports of Skotnicki *et al.* [4] and Serra et al. [5], the effect of stress configurations in FinFETs on the band alignment and mobility in Si can be discussed. Although a planar structure has been used in [4], the results can be applied to a 3D structure like a FinFET keeping in mind the importance of the aspect ratio in mind.

Fig. 5.1 shows a schematic cross section of the PiezoFET with two Si fins under applied bias across a homogeneously deposited PZT layer. The PiezoFET is basically a four terminal device consisting of two separate gates: the conventional gate which we call now the bottom gate (BG), and a top gate (TG, or “pigate”).

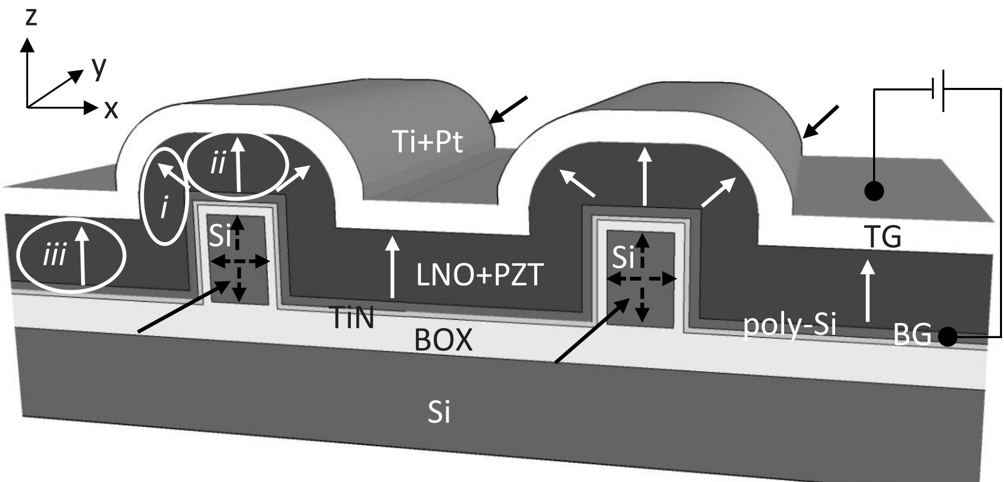


Fig. 5.1 PiezoFET schematic cross-section with narrow fins illustrating the formed strain condition corresponding to an upward piezoelectric response. The white arrows show the PZT deformation while the black arrows show the corresponding formed stress in the silicon fins. The figures are not to scale.

Fig. 5.1 shows the displacements when the PZT is poled in the direction of the electric field between BG and TG. The white arrows indicate the piezoelectric displacement and strain in the PZT layer, while the black arrows indicate the corresponding stress formed inside the Si fins. It is plotted such that the PZT on the BOX layer (and at the fin sidewalls) determines the net component.

This schematic is drawn when there is a negative bias over the PZT layer ($V_{\pi}= V_{TG}-V_{BG} < 0$ V). In this case, the stress formed in the Si fin can be described as follows: *i*) due to the PZT layer on the fin sidewall region, the Si fin is under biaxial tensile stress along *x* (fin width) and *z* (fin height) and under uniaxial compressive stress along *y* (channel length); *ii*) due to the PZT layer on top of the fin, biaxial compressive stress along *x* and *y* is formed and *iii*) due to the layer on the BOX region, tensile stress in Si along *x* and compressive stress along *y* is formed.

The overall effect depends on the fin width and aspect ratio. For narrow fin structures condition *i*) dominates whereas for a planar structure, condition *ii*) is more important due to a larger surface area. In practice, condition *iii*) would not be important for narrow fins, as will be explained later. For each fin width, the net stress depends on the amount of the individual stress components. For downward deflection (at positive bias over the PZT layer ($V_{\pi}= V_{TG}-V_{BG} > 0$ V)), all the stress components change direction.

While drawing this strain illustration, the stress relieving effect of the intermediate layers was not taken into account. Lower stress is expected when thick electrodes and intermediate layers are used for the same device configuration. In addition, stress does not form strain if the Si fin is clamped to the substrate, e.g. along the *y*-axis. On the other hand, the BOX layer is relatively soft and allows the Si fin to be stressed.

To increase the mobility, an optimum configuration needs to be found regarding the orientation of the channel with respect to stress (see chapter 1, Fig. 1.2). The FinFET geometry is important as well. In narrow fin devices the sidewalls dominate in determining the stress whereas for wide fins stress formed from the top of the fins is more profound. In general, wider fins have a lower amount of stress from piezoelectric actuation since the main stress component is formed by the PZT on the BOX that is a soft material [2].

To obtain high strain levels in Si, the stressor material needs to be as close as possible to the channel. This prevents stress relaxation due to the inter-layers. Stress also gradually decreases from top to bottom electrode in the PZT layer due to the clamping effect at the lower boundary. Therefore, the thickness and the choice of material between Si channel and PZT is very important. These have been optimized in the present state-of-art technology as described in chapter 3. The processing for the PiezoFETs has been carried out accordingly.

5.2 Processing of the PiezoFET

5.2.1 Mask design

Fig. 5.2 shows the schematic mask layout of a typical PiezoFET including its design parameters and table 5.1 gives an overview of the designed mask dimensions used in our studies.

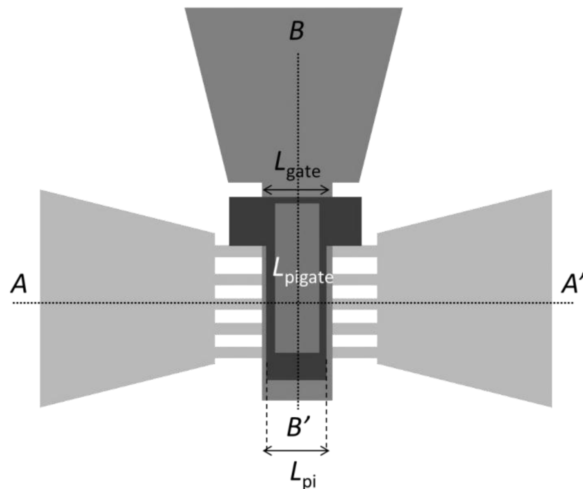


Fig. 5.2 Top view schematic layout of the PiezoFET with its design parameters. The figure is not to scale.

Table 5.1 *Summary of the designed PiezoFET mask dimensions. L_{gate}, L_{pi} and L_{pigate} represent the bottom gate length, piezoelectric layer length and top gate length, respectively.*

	L_{gate}	L_{pi}	L_{pigate}
PiezoFET-1	10 µm	8 µm	3 µm
PiezoFET-2	15 µm	13 µm	4 µm
PiezoFET-3	20 µm	18 µm	5 µm
PiezoFET-4	30 µm	28 µm	10 µm

Two different mask sets were designed for the fabrication. In the first design the piezoelectric layer dimensions were larger than the bottom gate. Using this mask set, the first PZT/LNO stack deposition and characterization experiments were carried out on FinFETs. The first observation was a serious underetch of the PZT layer, which would limit the top contact length. Moreover, if the PZT was patterned larger than the TiN (bottom) gate, the conductive LNO layer forms a short between the source (S) and drain (D) regions. Although the gate oxide layer on the S/D extensions of FinFETs should prevent this short, the dielectric properties deteriorated during the implantation or gate etching

processes. Therefore, a 2nd mask set was designed regarding these effects and presented in this section.

In the modified design (Table 5.1), the lateral dimensions of the piezoelectric layer (L_{pi}) have been kept larger than the top gate (L_{pigate}) because of the 2-3 µm lateral under etch of the PZT layer. However, although devices with four different gate lengths were designed, the ones with L_{pigate}= 3 µm and 4 µm were found to be leaky (PiezoFET-1 and 2). The small overlap between the top gate and piezoelectric layer could be the reason for the relatively high leakage between top and bottom gates. PiezoFET-3 and 4 were used in this work.

To compare the piezoelectric effect on FinFETs and on planar structures, test structures with different geometries and areas have also been designed. These structures are equivalent to the ones studied in chapter 3. Likewise, capacitors with different areas were designed including open and short de-embedding structures. The designed test structures consist of a so-called Ground-Signal-Ground (GSG) configuration, commonly used for high frequency measurements. Fig. 5.3 illustrates the designed test structures for planar *C-V* measurements as well as its de-embedding pairs. The top GSG pads are connected to the bottom (TiN) gate of the FinFET, while the bottom GSG pads are connected to the top gate. Table 5.2 summarizes the dimensions of the designed test capacitors.

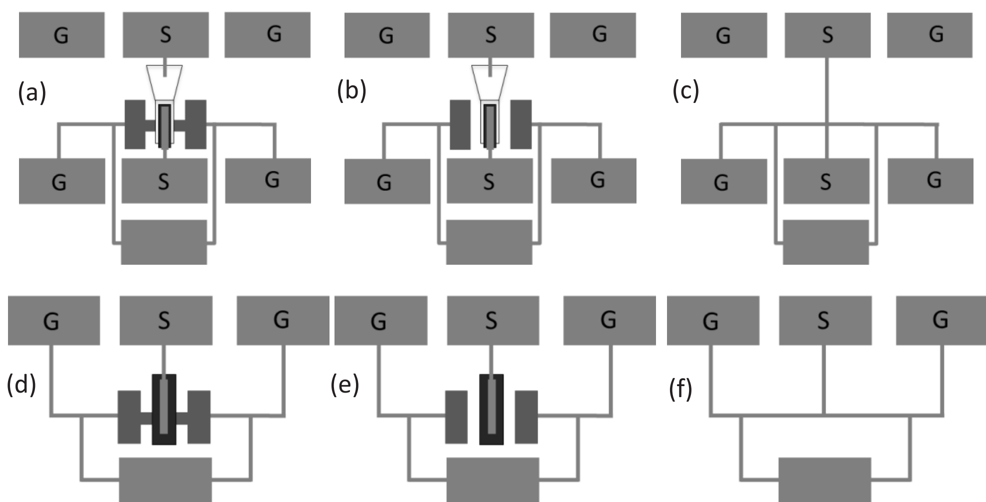


Fig. 5.3 Ground-signal-ground (GSG) *C-V* test structures for the *C-V* measurement of (a) the piezoelectric layer in an actual PiezoFET and its (b) open de-embedding, (c) short de-embedding structures; and those for *C-V* measurement of (d) the planar piezoelectric layer and its (b) open de-embedding, (f) short de-embedding structures.

Table 5.2 *Design parameters of the C-V test structures*

number of fins	W_{FIN}&L_{gate}& L_{pigate}	W_{FIN}&L_{gate}& L_{pigate}	W_{FIN}&L_{gate}& L_{pigate}
1	20 µm & 20 µm & 4 µm	10 µm & 20 µm & 4 µm	4 µm & 20 µm& 4 µm
20	20 nm & 20 µm & 4 µm	30 nm & 20 µm & 4 µm	40 nm & 20 µm& 4 µm
40	20 nm & 20 µm & 4 µm	30 nm & 20 µm & 4 µm	40 nm & 20 µm& 4 µm
60	20 nm & 20 µm & 4 µm	30 nm & 20 µm & 4 µm	40 nm & 20 µm& 4 µm

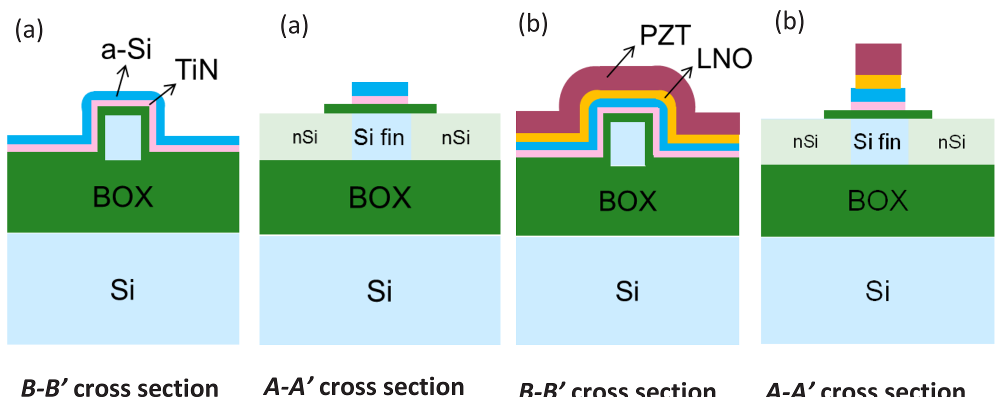
5.2.2 Processing

To fabricate the PiezoFET, the piezoelectric PZT layer was deposited on top of $(1\bar{1}0)/[110]$ oriented FinFETs, presented in chapter 4. The process scheme of the PiezoFET after the completed FinFET processing is depicted in Fig. 5.4.

(a) Al stripping

(b) LNO+PZT deposition & etching

(c) Metallization



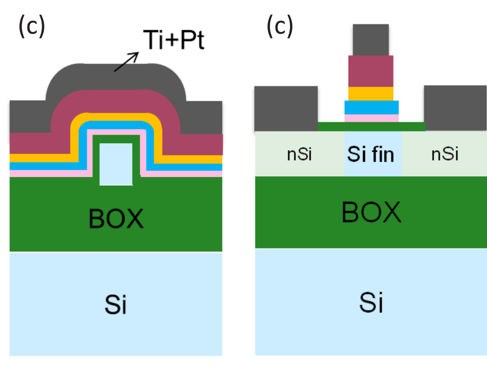


Fig. 5.4 Schematic process flow of the PiezoFET showing the process steps described in (a)-(c). The A-A' and B-B' cross sections are indicated in the top view schematic layout depicted in Fig. 5.2. The figures are not to scale.

The processing scheme can be summarized as follows:

(a) Al stripping: In this step, Al was stripped from the contacts pads since the PZT deposition temperature (650 °C) is not compatible with Al. The 250 nm Al was wet etched in standard phosphoric acid /acetic acid/nitric acid solution at 45 °C in 1 min. As mentioned in chapter 4, the metallization was done by using an Al-Si (1 %) target for the FinFET processing. Therefore, after Al removal, Si precipitates are still present in the contact regions.

(b) LNO+PZT deposition & etching: The $LaNiO_3$ (LNO) layer and the PZT layer were deposited in the pulsed laser deposition (PLD) system developed by SolMates BV, Enschede, the Netherlands. The deposition temperature was kept constant at 650 °C during the consecutive deposition of these layers. A 10 nm thick LNO layer and a 100 nm thick PZT layer were deposited (see Fig. 5.6). After deposition, further process steps were performed as described in chapter 3: the PZT/LNO stack was patterned by wet etching using a 2 step process: (1) 5 sec in BHF (12.5 %):HNO_3:NH_4Cl:H_2O (8:1:8:32) at room temperature and (2) 5 sec in HCl (45 %):H_2O (1:1) at 45°C. This 2 step process was repeated until the layer was completely etched. A 3 µm under etch of the PZT layer was observed through the optical microscope.

(c) Metallization: After patterning the contacts with photolithography (PL), the oxide on the contact holes was removed by 1 % HF etching. A 10 nm thick Ti and 100 nm thick Pt metal layers were sputtered as a contact metal. Then, a lift off process was done in acetone. In the final structure, all the contact pads are formed by a Pt/Ti stack, as shown in the optical micrograph of a PiezoFET in Fig. 5.5.

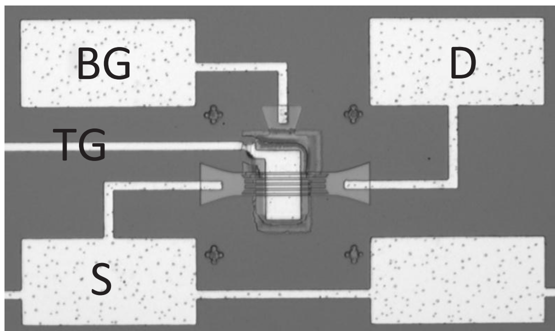


Fig. 5.5 Optical micrograph of a typical 5-fin PiezoFET. The bottom gate, top gate, drain and source are indicated by BG, TG, D, and S, respectively.

5.3 Physical, optical and ferroelectric characterization of PZT on FinFETs

5.3.1 TEM analysis

After sample preparation with the focused-ion beam system (FIB), cross section pictures were taken with a Transmission Electron Microscope (TEM). Fig. 5.6 shows TEM pictures of a 5-fin 20 nm and 100 nm wide PiezoFET with a 10 nm thick LNO and 100 nm thick PZT layer. All fins are imaged in Figs. 5.6 (a) and (d). Figs. 5.6 (b) and (e) show a magnified image of a single fin. The top gate is not visible in the figures due to the sample preparation (*i.e.* Pt protection layer). In this image, good step coverage of the TiN as well as poly-Si is recognized whereas the step coverage of the LNO/PZT stack is poor. This poor step coverage is due to the directional growth in the PLD system. This is obviously not an issue for the ALD deposition of TiN. Although the step coverage is poor, electrical measurements show that there is no direct electrical short circuit between the bottom gate (TiN) and the top gate Ti/Pt in the structures (see section 5.4.1).

To show each layer around the fin more clearly and to evaluate the crystal orientation of the PZT at the fin sidewalls, elemental as well as crystal analysis were done by the TEM. Figs. 5.6 (c) and (f) show the RGB (red, green, blue) map for the elemental analysis of a single fin. In this image, the La is shown in red; Ti is shown in green and Si is shown in blue. La is clearly observed on the top, while it gets thinner at the sidewalls of the fin. Figs. 5.6 (b) and (e) shows that the PZT layer thickness is decreased to 20-50 nm while the LNO layer thickness is decreased to 2-5 nm at the sidewalls. In Figs. 5.6 (g)-(h), a magnified image of the PZT layer at the sidewall and on top of the fin is shown. These images show that the PZT layer is poly-crystalline both at the fin sidewalls and on top of the fin.

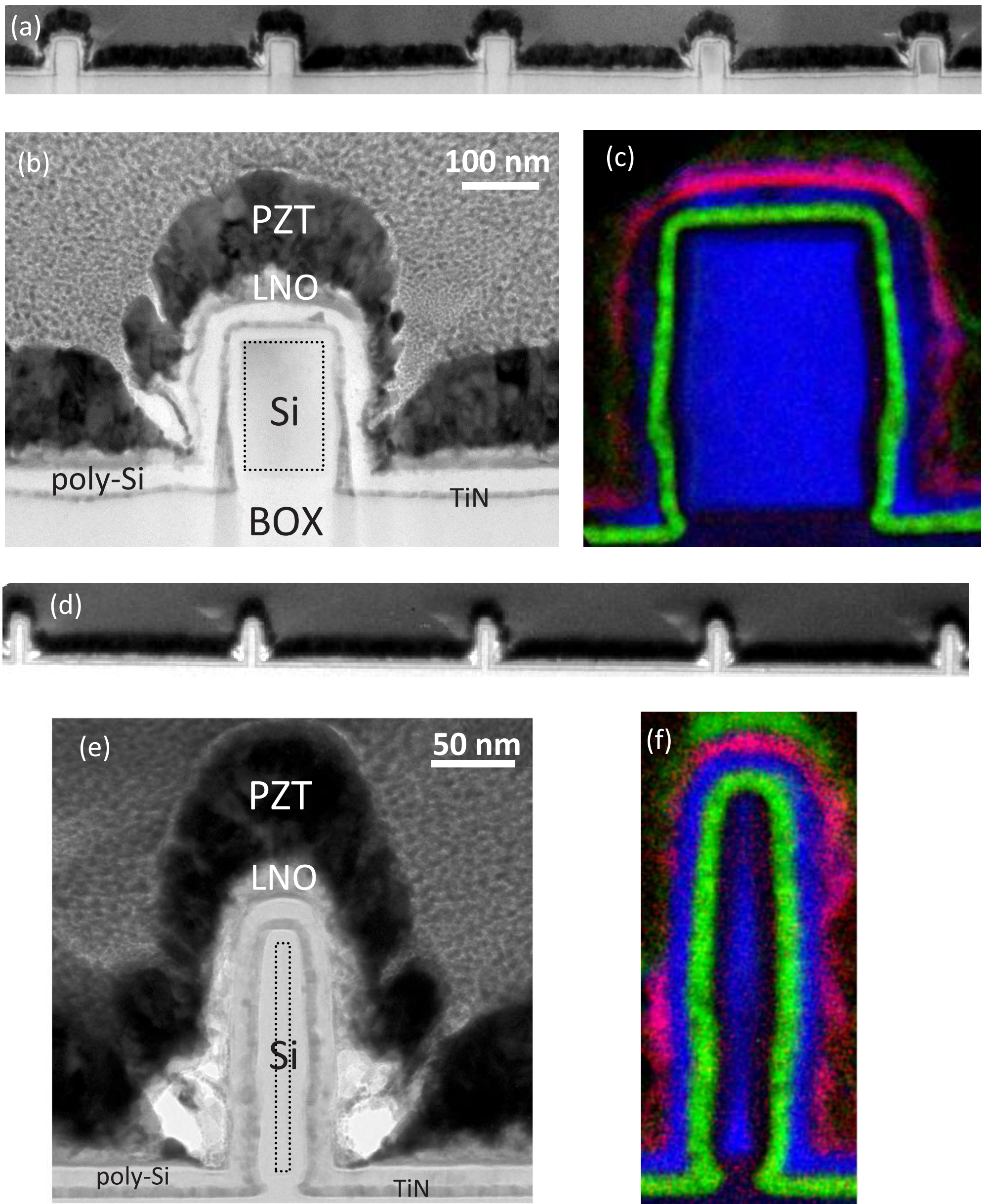

(a)
(b)
100 nm
PZT
LNO
Si
poly-Si
TiN
BOX
(c)
(d)
(e)
50 nm
PZT
LNO
Si
poly-Si
TiN
(f)

Fig. 5.6 HR-TEM images of a 5-fin PiezoFET with a 100 nm wide fin and a 10 nm LNO + 100 nm PZT layer stack: (a) zoomed out image of all fins, (b) magnified image of one fin (the dotted lines are drawn around the fin to guide the eye), (c) an RGB map of the fin (La, red; Ti, green; Si, blue), and with a 20 nm wide fin and a 10 nm LNO + 100 nm PZT layer stack: (d) zoomed out image of all fins, (e) magnified image of one fin (the dotted lines are drawn around the fin to guide the eye), (f) an RGB map of the fin (La, red; Ti, green; Si, blue), (g) magnified image of the PZT of the sidewall of the fin and (h) magnified image of the PZT on top of the fin. Figs. (g) and (h) are taken in the same direction as Figs. (b) and (e). They show that PZT is poly-crystalline both at the sidewall and top of the fin.

5.3.2 Laser Doppler vibrometer measurements

The laser Doppler vibrometer (LDV) measurement is important to characterize the piezoelectric response of the PZT layer, as was discussed in chapter 3. In chapter 3 the PZT layer was characterized on a planar surface while in this chapter analyses are presented on 150 nm high Si fins with different widths. This topography could have an effect on the piezoelectric and/or ferroelectric properties of the thin PZT layers compared to planar structures. In the LDV measurements, a 1 V dc and a 1 V sinusoidal ac-voltage at 8 kHz frequency were applied to a 100 nm thick PZT layer. The response under these measurement conditions is shown in Figs. 5.7 (a) and (b) for FinFETs with 30 nm and a 1000 nm fin width, respectively. Figs. 5.7 (c) and (d) show a line scan of the piezoelectric displacement across the dotted lines in Figs. 5.7 (a) and (b), respectively.

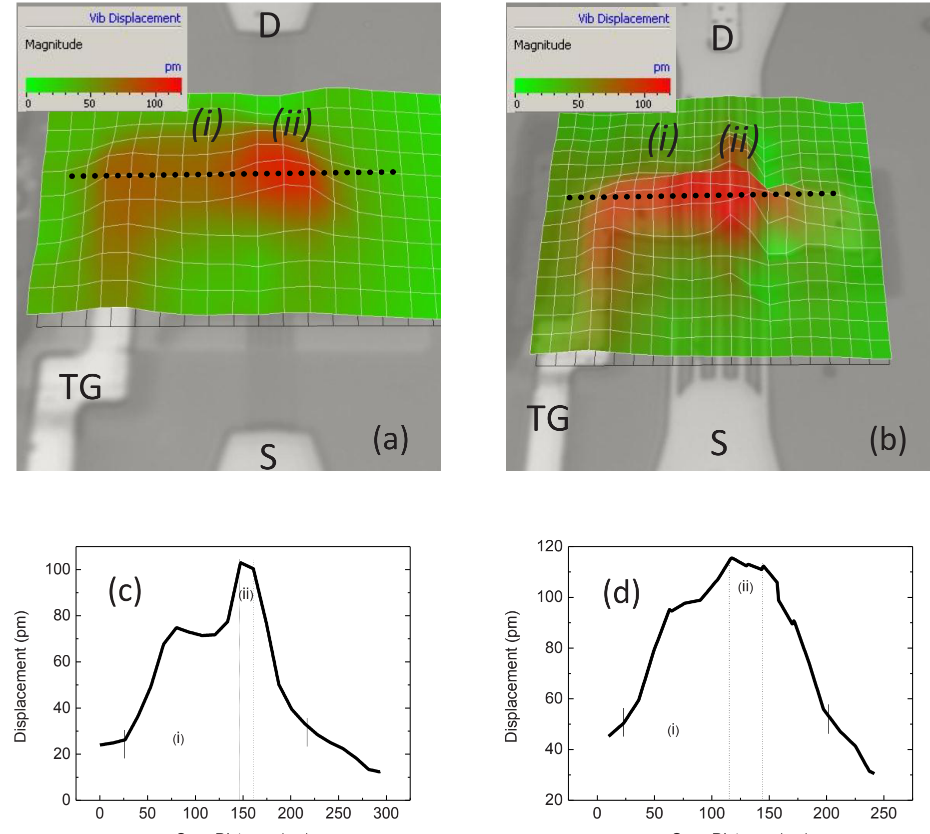


Fig. 5.7 2D upward response scans of a 5-fin PiezoFET with a (a) 30 nm and (b) 1000 nm fin width and L_{pigate}=10 μm, L_{gate}= 30 μm. Nominally 1 V dc and a 1 V ac voltage at 8 kHz frequency were applied to the film. The graphs in (c) and (d) are the line scan profiles of the displacement across the dotted line in (a) and (b). The channel response is indicated in between two vertical dotted lines. A 10 nm LNO+100 nm PZT film stack was used in this measurement.

The area where there is PZT between the TG and BG shows a clear displacement (Figs. 5.7 (a) and (b)). This is a strong indication of a piezoelectric effect. The displacement is enhanced on the FinFET channel. A piezoelectric coefficient of about $d_{33,f}$ =100-110 pm/V on the fin area and about $d_{33,f}$ =80-90 pm/V outside the fin area under the top contact has been determined. These values are obtained under a nominal voltage (1 V) applied over the PZT layer. As will be shown in section 5.4.1, the actual voltage drop over the PZT layer is less than the applied voltage. The values are doubled when the applied nominal AC voltage was increased to 2 V. This is an indication that the obtained displacement values are real displacement values.

Various explanations are possible to understand a higher displacement on the FinFET channel: *i*) thermal actuation as a result of increase in temperature due to high leakage

between the TG and BG (the cause of this high leakage will be explained in section 5.4.1.1), *ii*) transverse stress related local bending resulting in an amplitude increase, and *iii*) topography of the surface due to the fin height. Furthermore, there is a 10 % difference in the maximum displacement between the wide fin and narrow fin device. The maximum displacement is enhanced on wide fins possibly due to the relatively wide fin top surface, which is in the order of beam spot size and helps to obtain more signal from the fin top surface.

PiezoFETs with a 180 nm thick aluminum nitride (AlN) layer were also processed and an LDV analysis was performed on these devices. Piezoelectric activity was only observed for the 1000 nm wide devices. From the displacement data, $d_{33,f}$ value of 13 pm/V is calculated. Bulk AlN has a value around $d_{33} \approx 5$ pm/V [6, 7]. It shows that a higher displacement value than bulk value of AlN was obtained on the channel region. This is attributed to the mentioned reasons before.

5.3.3 Polarization hysteresis measurement

The polarization hysteresis (*P-E*) loop measurements of the PZT layer on a planar structure and on a FinFET were done using the same setup as described in chapter 3. The layers were also deposited under the same conditions as described in chapter 3. However, this time we could not obtain high polarization values on a planar structure for 100 nm thick PZT films, as shown in Fig. 5.8.

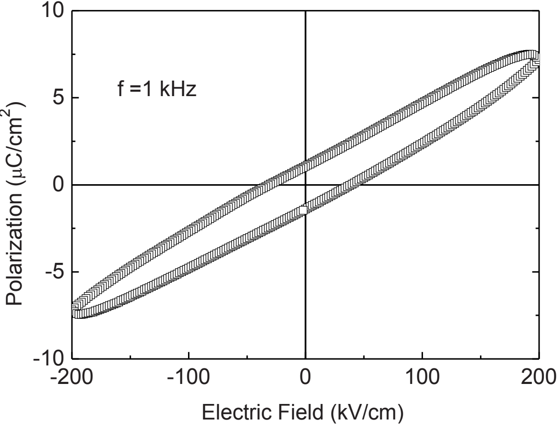


Fig. 5.8 Polarization hysteresis (*P-E*) loops of a planar PZT capacitor with a 50 µm x 50 µm area. The thickness of the PZT is 100 nm. The experiment was performed at the applied ac-electric field of ±200 kV/cm and 1 kHz frequency. The maximum applied dc bias was 2 V with the bottom gate grounded.

When the field was increased further, breakdown occurred. The leakage current was even higher in the non-planar structures (on FinFETs) and consequently no *P-E* loops could be obtained. The reason why the PZT layer on a planar surface has a higher leakage than the ones discussed in chapter 3 is probably due to (unintentionally) changed deposition conditions. Due to the relatively thin PZT layer at the fin edges, as shown in Figs. 5.6 (b) and (e), the electric field is higher and this results in higher leakage for the FinFET structures. We nevertheless expect that the PZT acts as a stressor because of the high displacement shown in section 5.3.2.

5.4 Electrical characterization of the PiezoFET

Studying the strain in PiezoFETs with optical strain characterization methods like Raman spectroscopy is a challenge. First, the Si channel will be strained when biasing the PZT layer. Therefore, the device needs to be biased during the optical analysis. Second, the PZT layer and the metallic layer on the PZT layer would strongly interfere with the laser signal.

The change in the band gap due to strain can be observed by the *I-V* characteristics of the device. In addition, the mobility can be calculated from the *I-V* curves. Since the change in mobility under stress is dependent on the stress level and the direction [4], any stress related effect can be recognized by electrical measurements. Therefore, *I-V* measurements were performed on PiezoFETs to recognize the effect of stress on the channels. The measurements were repeated using several devices with the same design parameters and it was found that they are reproducible.

5.4.1 Effect of PZT deposition on the I_d-V_{gs} curves

Single fin and 5-fin PiezoFET devices for different W_{FIN} were measured and analyzed. The schematic equivalent circuit is shown in Fig. 5.9. In the following discussion, a negative field over the PZT layer implies that a lower potential is applied to the top gate with respect to the bottom gate. All presented devices have a 100 nm thick PZT layer.

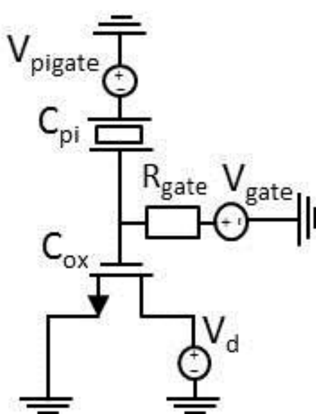
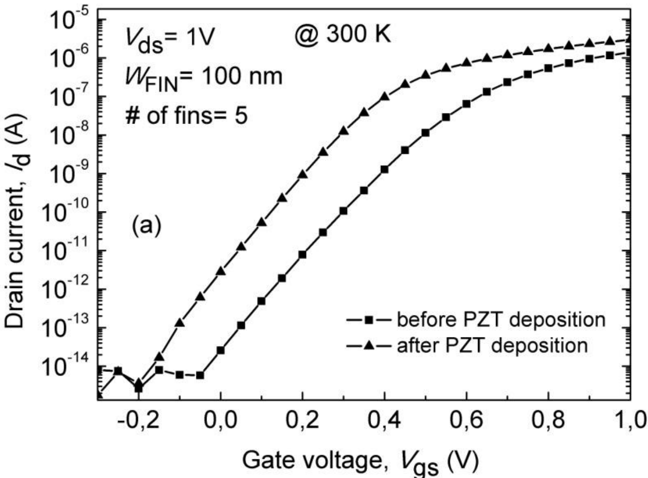


Fig. 5.9 Schematic equivalent circuit utilized for PiezoFET *I-V* measurements. To take into account its electro-mechanical properties, the piezoelectric capacitor C_{pi} is represented by an acoustic resonator symbol.

Fig. 5.10 shows the *I-V* curves of 100 nm wide fin devices before and after the 100 nm thick PZT deposition. A negative shift of threshold voltage (ΔV_{th}) as well as higher off current (I_{off}) is observed after PZT deposition. This voltage shift is observed in all of the devices. The largest shift is observed for the 1000 nm wide devices. Almost no degradation in the transistor characteristics is observed after deposition and processing of the LNO/PZT layers. The observed shift in the *I-V* curve could be due to stress in Si fin after the high temperature (650 °C) LNO/PZT PLD process.



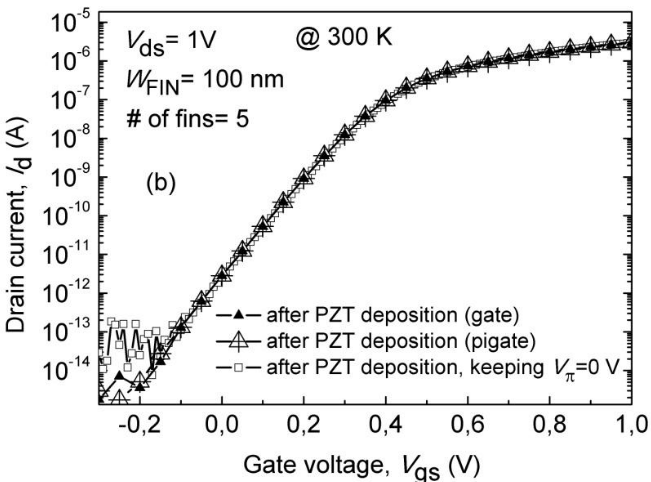


Fig. 5.10 I_d-V_{gs} device characteristics of a 5-fin devices with L_{pigate}=10 µm, L_{gate}=30 µm, W_{FIN}=100 nm at V_{ds}= 1 V and room temperature (a) FinFET before (closed squares) and after PZT deposition (closed triangles), (b) FinFET after PZT deposition (closed triangles), PiezoFET biasing the top gate, keeping the bottom gate floating (open triangles) and the same gate bas on the top and bottom gate (open squares).

It has been reported before that due to the difference in coefficient of thermal expansion (CTE) of the Si and PZT; a thermal stress can be developed in the PZT film [8]. Since Si has a CTE of 2.6 x 10^{-6} K^{-1} [9] and PZT has a CTE of 6.0x10^{-6} K^{-1} [10], additional thermal biaxial in-plane tensile stress is formed in the PZT film during the cooling down process from deposition temperature (650 °C) to room temperature. This will result in biaxial compressive stress in Si. Thermal expansion related stress profile and analysis has been reported before [11, 12].

The shift cannot be explained with the strain effect in the Si only since the observed shift of around 0.15 V is very large. Other possible reasons for this shift will be discussed in section 5.4.2.

Another important observation is that the *SS* is almost unchanged/only slightly reduced after the PZT deposition (which is more clearly observed in Fig. 5.17). More explanation on this subject will be given in section 5.4.2.

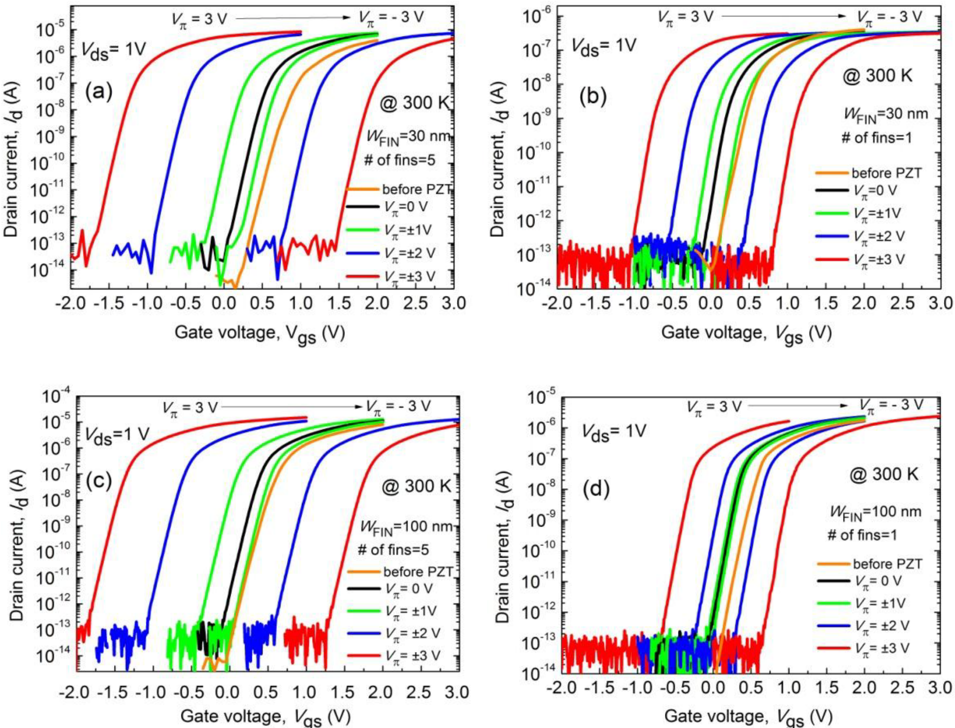
Fig. 5.10 (b) shows that the same I_d-V_{gs} curves are obtained irrespective when only the top gate (or pigate), or only the bottom gate is biased or when the piezoelectric layer is biased at zero volt. This means that there is almost no voltage drop over the PZT layer. To calculate the ratio of the voltage drop, the value of ε/t for the oxide and PZT layer has to be known. In chapter 3, ε_{PZT} was determined being 600 at zero volt. Therefore, ε_{ox}/t_{ox} is 11 times higher than that of $\varepsilon_{PZT}/t_{PZT}$. Hence, the voltage drop over the PZT layer is 11 times

less than that over the oxide. Therefore, we expect no difference in the I_d-V_{gs} characteristics of the device when operating with one gate only and leave the other one floating.

Furthermore, unlike reported for FerroFETs [13], no hysteresis behavior in our PiezoFETs is observed. Commonly, ferroelectric materials show hysteresis due to domain wall movements [14]. However, in our case, the relatively high leakage current interferes with the polarization switching and results in a non-hysteric behavior.

5.4.2 Effect of PZT biasing on the I_d-V_{gs} curves

In our further analysis, the PZT layer was biased at a constant and changing net bias between the top and (bottom) gate (V_{BG}=V_g) to observe the converse piezoelectric effect on the operation of the device (Fig. 5.11). The schematic of the measurement setup is shown in Fig. 5.9.



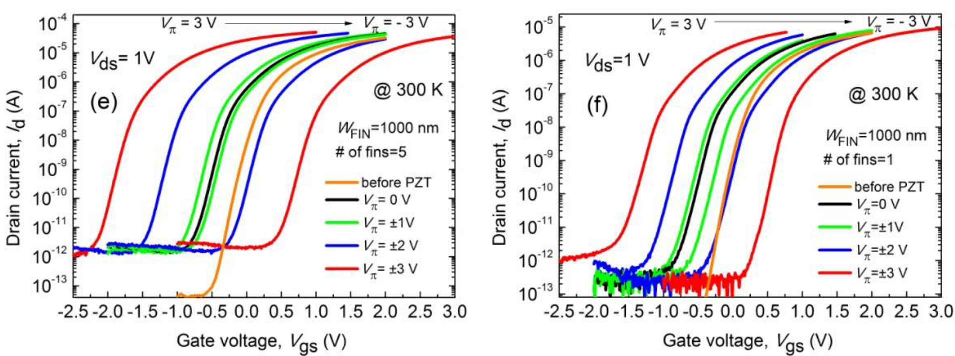


Fig. 5.11 I_d-V_{gs} device characteristics of the PiezoFETs for different V_π with (a) 5-fins with W_{FIN}=30 nm, (b) single fin with W_{FIN}=30 nm, (c) 5-fins with W_{FIN}=100 nm, (d) single fin with W_{FIN}=100 nm, (e) 5-fins with W_{FIN}=1000 nm, (f) single fin with W_{FIN}=1000 nm. All devices have L_{BG}=30 µm and L_{TG}=10 µm. The measurements were performed at room temperature.

First, a constant net bias was applied to the PZT layer and the device was measured by sweeping the bottom gate voltage. Figs. 5.11 (a) and (b) show the I_d-V_{gs} curves of 30 nm wide 5-fin and single fin PiezoFETs under 0 V, ±1 V, ±2 V and ±3 V constant net bias across the PZT layer (V_π). For zero bias over the PZT layer, a large negative shift is observed for both devices. A negative shift is also observed under positive bias whereas a positive shift is observed under negative bias. The threshold voltage shift is increased when V_π is increased. However, single fin devices show a smaller shift (see also Fig. 5.14). Figs. 5.11 (c)-(f) present the similar measurements of 5-fin and single fin device structures with 100 nm and 1000 nm fin widths. Note that, to check the reproducibility of this effect, another wafer was processed and the same PiezoFETs were measured. We observed a similar behavior for these devices as well.

These devices can be utilized to combine low V_{th}, low I_{off} and steep sub-threshold swing (*SS*). In order to do so, I_d-V_{gs} device characteristics can be measured under an increasing net bias over the PZT layer In Fig. 5.12 I_d-V_{gs} curves of a 5-fin device with W_{FIN}=30 nm are plotted at changing V_π from 0 V to 1 V, 2 V and 3 V during the gate sweeping. By increasing the V_π from 0 V to 3 V, the *SS* was decreased from 74 mV/dec to 48 mV/dec. Therefore, with the help of the threshold voltage shift effect and by tuning V_π, a low *SS* can be obtained. Although there is a power drawback due to a need for V_{TG}>V_{gs}+1 and the leakage current, this figure shows that *SS* can be modified by controlling the gate biases.

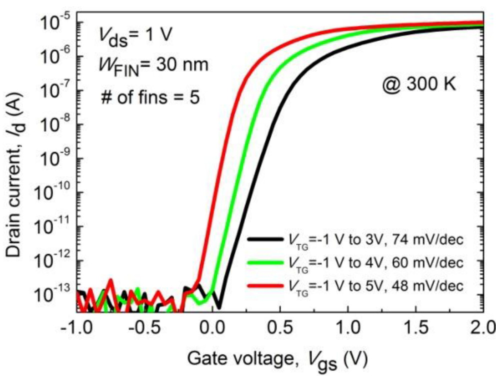


Fig. 5.12 I_d-V_{gs} device characteristics of a 5-fin, W_{FIN}= 30 nm device at V_{TG} changing from -1 V to 5 V while V_{gs} (=V_{BG}) is sweeping from -1 V to 2 V. Device have L_{BG}= 30 µm and L_{TG}= 10 µm. The measurements were performed at room temperature.

Fig. 5.13 shows the ΔV_{th}-V_{π} curves for the devices presented in Fig. 5.11. There is an exponential dependency of the ΔV_{th} on the applied bias, reaching +1.5 V and -2 V under -3 V and +3 V applied bias over PZT, respectively. There is also an asymmetry regarding the polarity. In addition, as mentioned before, 5-fin devices show a larger shift than 1-fin devices. For a single fin device, the largest shift seems to occur for the 30 nm fin width. A device with a shorter gate length is also plotted in the same figure to show that there is small dependency of ΔV_{th} with the bottom gate length.

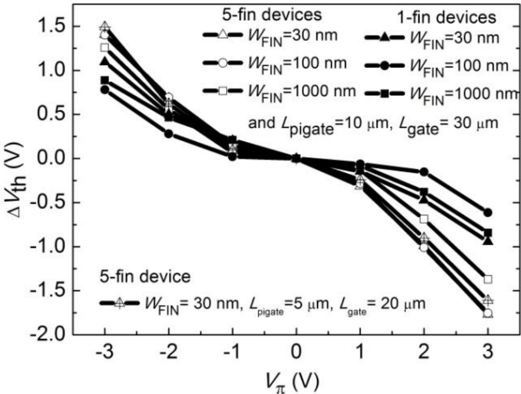


Fig. 5.13 ΔV_{th}-V_{π} curve of 5-fin and single fin PiezoFET devices with a 30 nm, 100 nm and 1000 nm fin width. Devices have L_{BG}= 30 µm and L_{BG}= 10 µm, except for one device with L_{BG}= 20 µm and L_{TG}= 5 µm.

In Fig. 5.14 the J-V_{π} characteristics of the PZT capacitor on devices with different fin widths as well as on a planar surface are plotted.

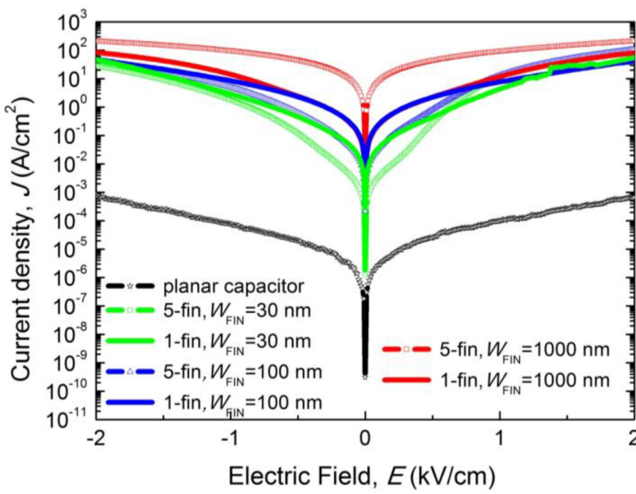


Fig. 5.14 J-V_{π} characteristics of the PZT capacitor on a planar surface and on 5-fin and single fin FinFETs. L_{TG}= 10 µm for all devices.

The leakage current of the PZT and the ΔV_{th} (Fig. 5.13) of the PiezoFET show an exponential dependency on the applied bias. The leakage current of the PZT capacitor is high on planar surfaces compared to that obtained for the planar PZT capacitors discussed in chapter 3. The leakage current is, however, much higher when integrated with FinFETs. Typically, the leakage currents show a symmetric behavior similar to those of the planar structures as discussed in chapter 3. In general, single fin devices show less leakage than 5-fin devices above certain fields. However, the leakage current does not scale linearly with the number of fins. The main issue remains to be the step coverage of the PZT layer around the fins.

PiezoFETs with a 180 nm thick AlN layer were deposited and measured for comparison. Figs. 5.15 (a)-(c) show the I_d-V_{gs}device characteristics of the AlN PiezoFET with a 180 nm thick AlN layer.

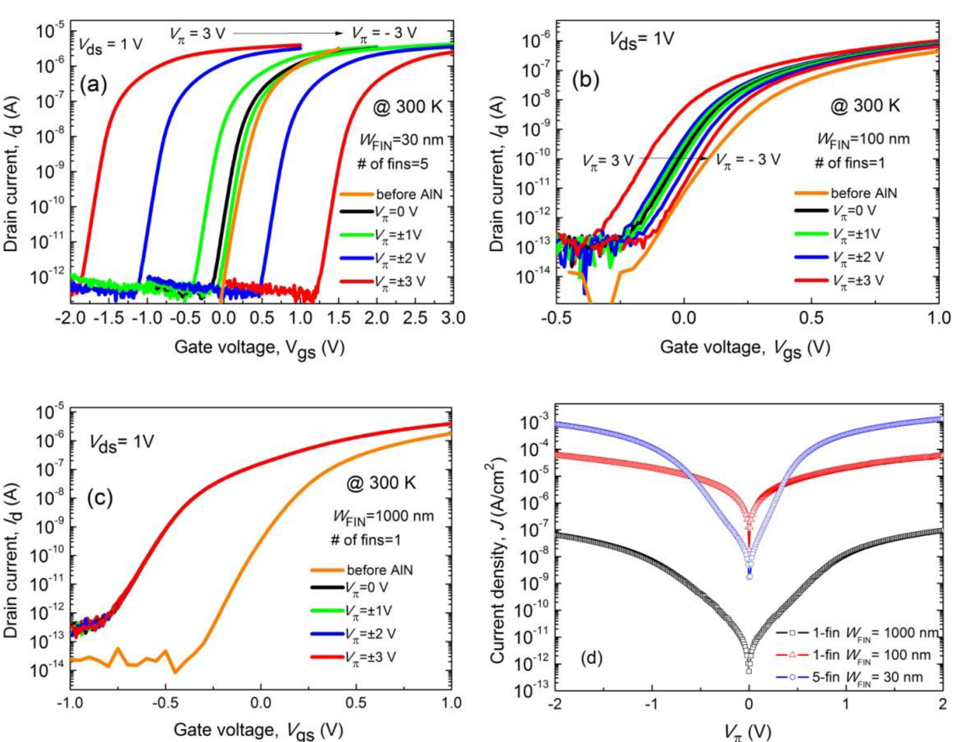


Fig. 5.15 I_d-V_{gs} device characteristics of the AlN PiezoFETs for different V_π with (a) 5-fins with W_{FIN}= 30 nm, (b) single fin with W_{FIN}= 100 nm and (c) single fin with W_{FIN}= 1000 nm. The leakage current density of AlN is plotted in (d) corresponding to devices plotted in (a)-(c). All devices have L_{BG}= 30 µm and L_{TG}= 10 µm. The measurements were performed at room temperature.

Similar to the PZT deposited devices, a negative shift in the threshold voltage is observed after AlN deposition without any bias. The amount of shift is smaller compared to devices with PZT layer in Fig. 5.11. The strain formed due to the difference in CTE is regarded as the reason for this shift. The CTE of AlN is smaller than PZT and the deposition temperature is lower, i.e. lower strain is expected. Again, the largest shift occurs for the 1000 nm wide device.

The AlN PiezoFET with 5-fins of 30 nm fin width shows the same amount of shift under applied bias compared to a PZT PiezoFET with the same dimensions (see Fig. 5.11 (a)). However, for a fin width of 100 nm (Fig. 5.15 (b)), the shift is smaller for the AlN PiezoFET. When the fin width is 1000 nm (Fig. 5.15 (c)), no shift is observed. The measured leakage current of AlN on devices is given Fig. 5.15 (d). In this case, a single fin 1000 nm wide device has five orders of magnitude lower leakage current than a 30 nm wide 5-fin device at 2 V. The shift proportionally decreases with the leakage current and this is a clear indication that the threshold voltage shift is related to the leakage current through the piezoelectric layer, which is most probably higher at the fin sidewalls.

This threshold voltage shift can be explained by an electrical DC equivalent circuit diagram of a leaky piezoelectric capacitor on top of the FET connected by the (bottom) gate resistance. A ΔV_{th} is expected when the bottom gate resistance is comparable with the resistance of the piezoelectric layer. The corresponding schematic equivalent circuit is shown in Fig. 5.16.

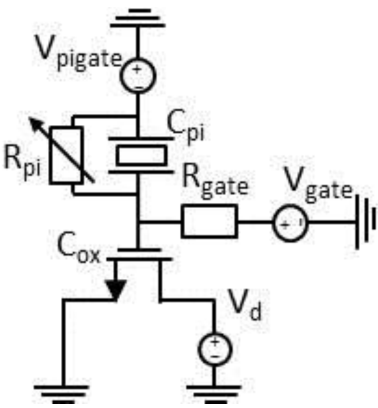


Fig. 5.16 Modified schematic equivalent circuit of the measurement setup utilized for the PiezoFET *I-V* measurements.

In the ideal case (Fig. 5.9), there is no current through the piezoelectric capacitor C_{pi} and the surface potential on the gate is V_{gate}. However, when there is a (variable) resistor (R_{pi}) parallel to the piezoelectric capacitor (Fig. 5.16), the surface potential will be influenced. The influence of R_{pi} on the surface potential is determined by the relative values of R_{gate} and R_{pi}.

The resistivity and thickness of the TiN external connection to the bottom gate is 160 µΩ-cm and 6 nm, respectively (see chapters 3 and 4). The length of this connection is 50 µm and the width is 30 µm. This yields a resistance of R_{gate}= 445 Ω. The leakage current of the PZT capacitor deposited on the 1000 nm wide single fin device was 2.5 mA at V_{π}= 3 V. Therefore, by calculating the real (internal) voltage drop over the PZT layer, we obtain a PZT resistance value of about 755 Ω.

According to the calculated values of resistances, ≈ $2/3 \cdot V_{\pi}$ has dropped across the PZT layer whereas the rest of the voltage drop is across the gate. The surface potential is increased by this amount and therefore, a threshold voltage shift occurs. It is observed in Fig. 5.13 that under a 3 V bias, the threshold shift is about 0.9 V for 1000 nm wide single fin device. This value is 1.11 V, very close to the calculated voltage drop over the gate. Since we do not account for distribution effects caused by current spreading on top of the channel region, the calculated resistance value is an approximation. On the other hand, the 1000 nm fin width device with the AlN layer shows low leakage (Figs. 5.15 (c) and (d)), the R_{pi} is high and the surface potential is less affected.

In summary, the observed threshold voltage shift in our devices is a result of the piezoelectric layer leakage current. This section will continue with the PZT deposited PiezoFETs.

To observe the effect of V_π (=V_{TG}-V_{BG}) on the sub-threshold region, *SS*-V_π graphs of PZT deposited PiezoFETs are plotted in Figs. 5.17 (a) and (b).

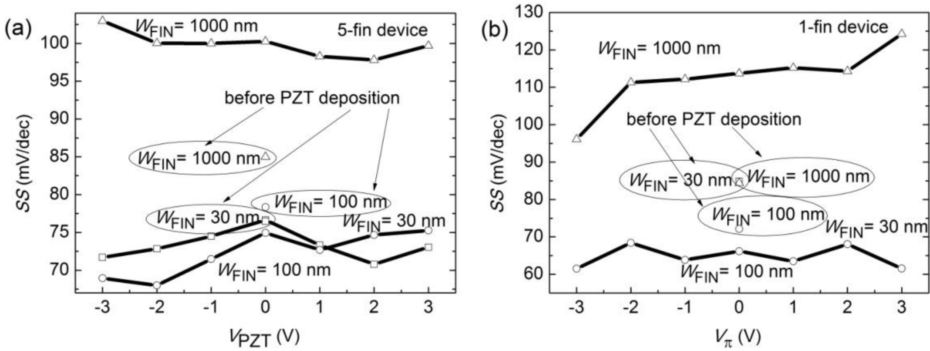


Fig. 5.17 *SS*-V_π graph of (a) 5-fin, (b) 1-fin devices with W_{FIN}= 30, 100 and 1000 nm at V_{ds}= 1V. All devices have L_{BG}= 30 µm and L_{TG}= 10 µm.

The *SS* values are above 60 mV/dec indicating presence of interface traps, in particular for the narrow fin devices. Fig. 5.17 also shows that the *SS* is decreased (reduced effective interface trapping of charge carriers) for devices with 30 nm and 100 nm fin width after PZT deposition and without biasing. Up to 20 % improvement in the *SS* is observed after the PZT deposition. It could indicate that the gate oxide (SiO_2) layer has been stressed along its interface with the Si body, possibly affecting the band alignment. The effect of fixed strain on the trapping probability and band modulation was reported before [15, 16]. This work reports it on our tunable strain devices as well.

Stress in the oxide layer can be a reason for the slightly reduced *SS* and possibly a part of the observed threshold voltage shift. Since the SiO_2 is less stiff than Si, most of the strain will be absorbed in the oxide. For instance, the FEM simulations of the NXP FinFETs discussed in chapter 2 predict higher strain values in the gate dielectric than in the Si body (Fig. 2.3).

For the 1000 nm wide fin sample, however, *SS* increased. This is possibly due to its different crystal orientation. Wide fin devices have a (001) surface orientation, instead of the $(1\bar{1}0)$ surface sidewall orientation dominant for narrow fin samples. The available bonds for (001) surface is smaller than $(1\bar{1}0)$ surface. That would change the density of interface states. In addition, as will be mentioned later in section 5.4.3.1, we expect a different stress configuration for wide and narrow fins. This would have a different effect on the band alignment.

The reduction of the *SS* for narrow fins indicates a decrease of the interface trap density. For wide fins, however, the *SS* increases and this indicates an increase in the interface trap density (Table 5.3). Furthermore, the *SS* is modified slightly (up to 10 %) by biasing the PZT layer on the 5-fin devices. For a 5-fin device with 30 nm and 100 nm fin width, the *SS* is slightly decreased with an applied PZT bias (Fig. 5.17 (a)). There is almost no trend in *SS* for single fin devices with the same fin width (Fig. 5.17 (b)).

The interface trap density, D_{it}, has been calculated as described in section 4.2.3. Table 5.3 shows the calculated D_{it} values for the 5-fin devices presented in Fig. 5.17 (a). For 30 nm and 100 nm wide fins, biasing the PZT decreases the trap density. The D_{it} values under PZT bias are not given for 1000 nm wide fins due to the interference of high leakage current due to short channel effects.

Table 5.3 D_{it} values calculated from the minimum *SS* values in Fig. 5.17 (a).

W_{FIN} (nm)	D_{it} before PZT (1/eV-cm^2)	D_{it} at $V_\pi = 0$ V (1/eV-cm^2)	D_{it} at $V_\pi = 3$ V (1/eV-cm^2)	D_{it} at $V_\pi = -3$ V (1/eV-cm^2)
30	$5.23\text{x}10^{11}$	$5.37\text{x}10^{11}$	$4.21\text{x}10^{11}$	$3.78\text{x}10^{11}$
100	$5.92\text{x}10^{11}$	$4.82\text{x}10^{11}$	$4.93\text{x}10^{11}$	$2.88\text{x}10^{11}$

Since a high piezoelectric response was obtained on top of the device structures (section 5.3.3), a certain amount of strain is expected in the underlying layers. Changing V_π, i.e. strain, will change the mobility. The following section discusses the effect of strain on the mobility in FinFET devices. The threshold shift has been taken into account in mobility extraction. Therefore, it is expected that it does not affect the obtained results.

5.4.3 Mobility calculations

The effective electron mobility of the PiezoFET has been calculated in the same way as described in chapter 4 and hence the effect of the ΔV_{th} has already been compensated for. Fig. 5.18 shows the effective electron mobility as a function of the electric field (μ_{eff}-E) for 5-fin and single fin $(1\bar{1}0)/[110]$ PiezoFET devices with W_{FIN}= 30 nm, 100 nm and 1000 nm for different V_π. For comparison, the μ_{eff}-E curves of the (100) bulk MOSFET (Fig. 5.18 (a)) and the (110) FinFET and the (110) bulk MOSFET (Fig. 5.18 (e)) are also shown [17, 18].

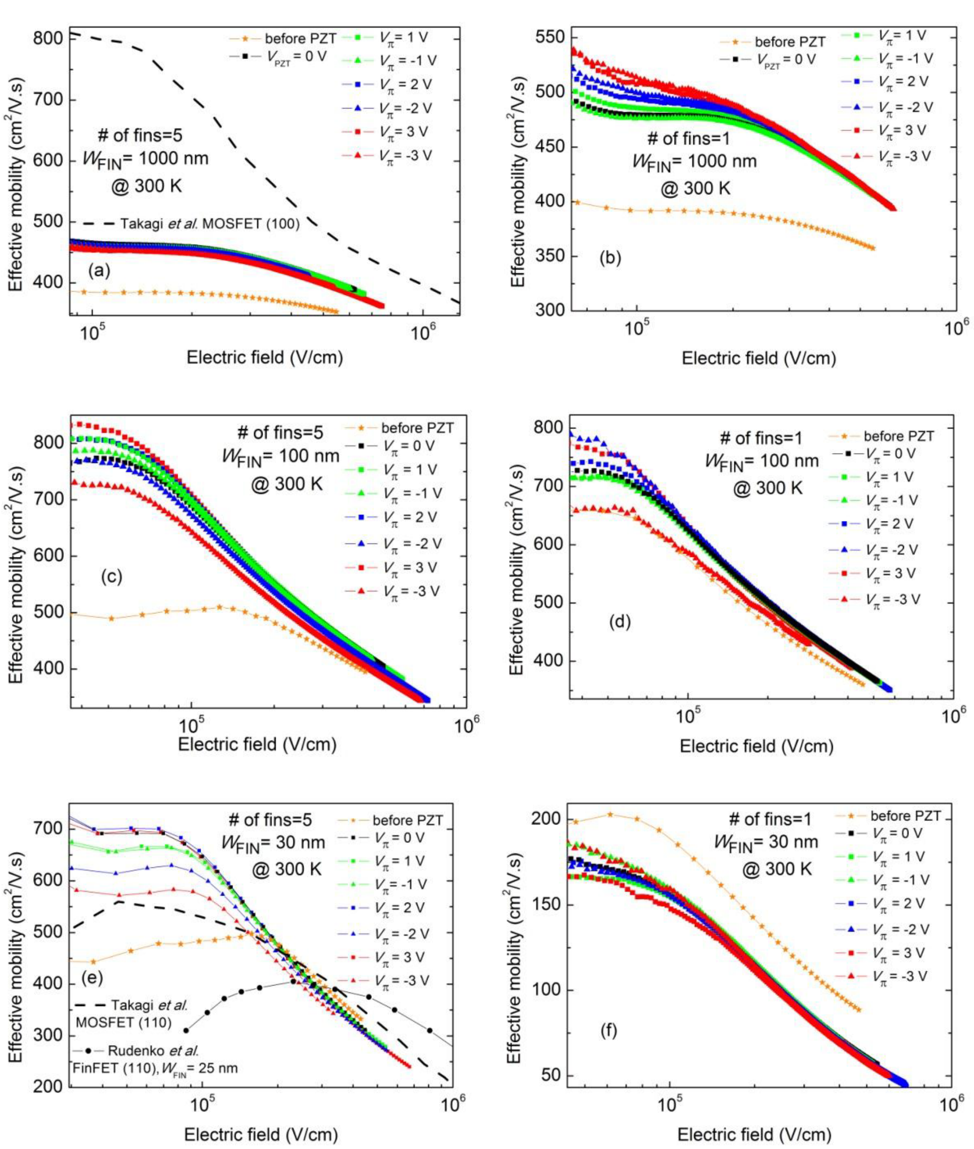


Fig. 5.18 Effective electron mobility-electric field curves of PiezoFETs for different biasing over the PZT layer with (a) 5-fins of W_{FIN}=1000 nm and (100) MOSFET obtained from Takagi *et al*. [17], (b) a single fin of W_{FIN}= 1000 nm, (c) 5-fins of W_{FIN}= 100 nm, (d) a single fin of W_{FIN}= 100 nm, (e) 5-fins of W_{FIN}= 30 nm and (110) FinFET with W_{FIN}= 25 nm obtained from Rudenko *et al*. [18], (110) MOSFET obtained from Takagi *et al*. [17], (f) a single fin of W_{FIN}= 30 nm (T=300K). All devices have L_{BG}= 30 µm, L_{TG}= 10 µm. All measurements were performed at 300 K.

Up to ≈ 20 % increase in the mobility was observed after PZT deposition on 1000 nm wide 5-fin and single fin devices (Fig. 5.18 (a) and (b)). The effect on 100 nm and 30 nm wide 5-fin devices at low fields is stronger; up to ≈ 50 % increase in mobility (Fig. 5.18 (c) and (e)). For high fields, no significant change is observed. The single fin device with 100 nm fin

width show up to 8 % increase in mobility (Fig. 5.18 (d)). The mobility is decreased by about 12 % for a single fin device 30 nm fin width (Fig. 5.18 (f)).

The change in the mobility, however, is smaller for varying V_π. The μ_{eff} is affected up to ≈ 20 % by the voltage V_π between the top and bottom gate. Compared to the mobility values given in literature [18], the low field mobility is higher whereas the high field mobility is lower in our devices. The higher mobility at lower fields is an indication of less effective Coulomb scattering (which has an effect on mobility in this region), most probably because of a higher fin and the use of SiO_2 as a gate dielectric in our case. In [18], a high-κ material has been used in which dipoles that are close to the channel could increase the Coulomb scattering. However, the lower mobility at higher fields is an indication of more surface imperfections in our devices.

The mobility in devices with deposited AlN was also calculated for comparison. An increase in mobility after AlN deposition was also observed. The most significant change is obtained again for 1000 nm wide devices. Biasing of the AlN layer showed no significant change in the mobility. This is expected due to a lower piezoelectric response of the AlN compared to that of PZT.

To show the trend in the mobility more clearly when biasing the 5-fin and single fin PZT PiezoFETs, the mobility-V_π curve has been plotted when biased at moderate inversion (Fig. 5.19) and at strong inversion (Fig. 5.20). For the 30 nm and 100 nm wide fin devices, the applied fields are at E= 5x10^4 V/cm and E= 2x10^5 V/cm for moderate and strong inversion, respectively. Due to the fact that the W_{FIN}= 1000 nm device act as a partially depleted SOI device, a higher electric field is needed to obtain strong inversion. Therefore, for a 1000 nm wide device, the effective mobility-V_π curve is plotted at a higher field of 1x10^5 V/cm and 4x10^5 V/cm for moderate and strong inversion, respectively.

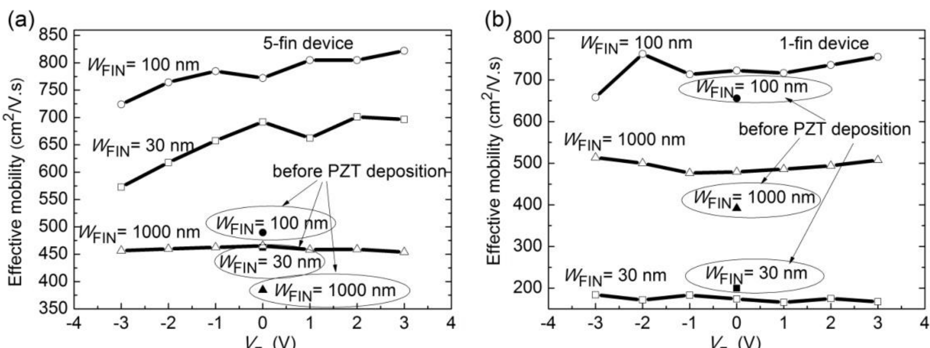


Fig. 5.19 Effective electron mobility-V_π curves of devices at a 5x10^4 V/cm field for 30 nm and 100 nm wide fin devices and at a 1x10^5 V/cm field for a 1000 nm wide fin device for (a) 5-fins and (b) a single fin.

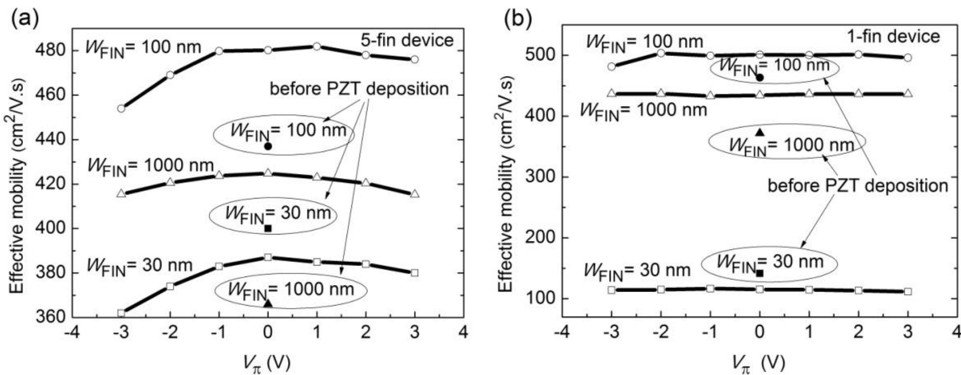


Fig. 5.20 Effective electron mobility-V_π curve of devices at a $2\text{x}10^5$ V/cm field for 30 nm and 100 nm wide fin devices and at a $4\text{x}10^5$ V/cm field for a 1000 nm wide fin device for (a) 5-fins and (b) a single fin.

At low fields, the effective mobility shows an increasing trend under positive applied bias and decreasing trend under negative applied bias for 30 nm and 100 nm wide devices with 5-fins. Single fin devices show no clear trend. At high fields, mobility decreased again under negative applied bias. But no trend is observed for positive applied bias. Single fin devices show no clear trend again. The next step is to discuss the possible reasons for the observed mobility behavior.

5.4.3.1 Discussion

First, the effect of the deposition of the PZT layer on the electron mobility will be discussed. Second, we discuss the effect of strain induced by the converse piezoelectric effect on the electron mobility. Before the discussion, several things should be kept in mind:

1) It should be emphasized that stress related effects do not impact the electron mobility in the same way for weak inversion and strong inversion [4]. The increase of mobility by strain will be enhanced by an increase of the relaxation time due to reduced intervalley scattering in weak inversion. This is because of the reduction in the amount of conduction band valleys, the so-called degeneracy, which contributes to the current. In addition, the electrons in the inversion layer are strongly confined. The quantization effect is known to counteract the stress induced repopulation of the electron valleys [5]. At strong inversion this confinement strongly depends on the applied bias contrary to weak inversion. Therefore, we observe a different behavior in the strong and moderate inversion regimes.
2) In addition to point 1), in the moderate inversion (*i.e.* near threshold voltage) regime Coulomb scattering is important for the mobility. This type of scattering is affected by ions present in the silicon body or at the interface, but by effective interface traps as

well ($\mu_{ic} \propto {}^{1}/_{N_{it}}$, with N_{it} is the amount of traps) [19]. For strong inversion, another non-ideal effect such as surface scattering is important: $\mu_{sr} \propto {}^{1}/_{(\Delta L)^2}$, with Δ is the surface deviation perpendicular to the surface flatness, and L is the lateral length scale of the roughness fluctuations [20, 21]. However, surface scattering is less important for narrow fins (see chapter 1).

3) As mentioned before, when we were illustrating the strain effect, we neglected the strain relieving effect of the intermediate layers between the PZT layer and the Si fins. Also, effects such as non-uniformity caused by poor step coverage of several layers along the fin perimeter were not taken into account. Either way these issues will not dramatically affect the conclusions drawn from this qualitative discussion.

After deposition (before applied bias) of the PZT layer:

As shown in Figs. 5.19 and 5.20, the mobility has increased for 1000 nm and 100 nm wide fin devices with 5-fins and a single fin after the LNO/PZT deposition for V_{π}= 0 V. The mobility has decreased for a 30 nm wide fin device with 5-fins and a single fin for high fields (Figs. 5.20 (a) and (b)). Only the 5-fin device shows higher mobility values at lower field in Fig. 5.19 (a) (in the moderate inversion regime when Coulomb or ion scattering is important) after PZT deposition. The difference in the effective mobility and the shift in the threshold voltage in the *I-V* curves indicate that strain is formed after deposition of the LNO/PZT stack. Furthermore, as mentioned before, oxide deformation after PZT deposition can possibly change the interface trap density. At low field, Coulomb scattering is important and that is affected by the traps. Therefore, oxide deformation can also help to increase the low field mobility.

At high fields on the other hand surface roughness scattering is important which could also be affected by strain. As discussed in section 5.4.1, we expect biaxial tensile stress in the PZT due to difference in CTE when no external bias is applied. As shown in Fig. 5.6, the step coverage of the PZT is not as ideal as depicted in Fig. 5.1. Therefore, we expect that the stress profile is not determined by the PZT layer on the BOX layer, but more by the PZT layer located at the fin sidewall. Therefore, for narrow fins ($W_{FIN} \ll H_{FIN}$), a strain gradient parallel to the surface of the $(1\overline{1}0)$ fin sidewall is important. In this case, for narrow fins, biaxial compressive stress along the fin height and channel length direction is formed. This results in uniaxial tensile stress along the fin width direction and consequently increases high field electron mobility [5].

For narrow fins under both tensile and compressive stress along the fin height direction, the conduction band valleys move down in energy. The latter would give a larger impact both in the band offset and increased mobility [5]. This will result in a negative threshold

voltage shift after deposition [2]. This can cause a relatively small part of the shift in threshold voltage observed in Fig. 5.10 (a).

Compressive stress along the fin height direction move the Δ_2 ("light") electron valleys down in energy. The conductivity effective mass of electrons reduces, thereby increasing the electron mobility. Since we expect compressive stress along the channel length, this stress configuration is present for narrow fins in our devices (for W_{FIN}= 30 and 100 nm). We can observe it in Fig. 5.19 (a) at low field (moderate inversion) region.

For wide fins (W_{FIN}>>H_{FIN}) on the other hand, the sidewalls can be neglected compared to the top surface of the fin. Therefore, wide fins are expected to behave like a planar (001) surface (as in a (001) bulk MOSFET). Since the Si substrate is much thicker than the Si fin height, the intermediate layers and the PZT layer, the in-plane biaxial tensile stress formed in the PZT layer will be transferred to the underlying layers down to the Si substrate [22]. Hence, biaxial tensile stress along the fin width and channel length direction is formed. This configuration would result in uniaxial compressive stress along the fin height direction.

Compressive stress along the fin height direction move Δ_2 ("light") electron valleys down in energy. The conductivity effective mass of electrons decreases and thereby electron mobility increases. This stress configuration is present for wide fins in our devices (for W_{FIN}= 1000 nm) which is (001) surface oriented. This can be seen in Fig. 5.19 and 5.20 (a)-(b).

In summary, before any V_π biasing, the low field mobility (moderate inversion) increases possibly by the oxide deformation that reduces the effective interface traps at the Si/SiO_2 interface. On the other hand, the CTE difference formed strain in Si influences the high field mobility (strong inversion). For wide fins, the high field mobility increases due to biaxial tensile stress along the fin width and channel length direction in the (001) surface. For narrow fins, the mobility also increases due to biaxial compressive stress along the fin height and channel length direction in the $(1\bar{1}0)$ surface of the fin sidewall.

Biasing the PZT layer:

A bias varying from -3 V to 3 V has been applied over the PZT layer and the mobility has been calculated. According to Fig. 5.1 (a), we expect upward deflection under negative whereas downward deflection under a positive applied field [23]. Therefore, for a negative field, we expect the narrow Si fin to be more compressively stressed along the channel length direction and tensile stress in fin height direction and the mobility decreases. On the other hand, for a positive field, more tensile stress is formed along the channel length direction and compressive stress in fin height direction and the mobility increases [5]. For a wide fin the situation is different. When applying a positive applied

field we have biaxial tensile stress at the (001) surface which tends to increase the electron mobility [4]. On the other hand, a negative bias will yield almost no change in the mobility.

At low field: Fig. 5.19 (a) shows an increasing trend of the effective mobility of up to 20 % at a positive bias for 30 nm and 100 nm wide fins. The trend is the opposite at a negative applied bias. For the 1000 nm wide device however, there is almost no change. Fig. 5.19 (b) shows that there is almost no change in mobility for single fin devices. Therefore, the trend of mobility for 5-fin 30 nm and 100 nm wide devices can be explained by data from literature.

At high field: In Fig. 5.20 (a) a smaller decrease in effective mobility at a negative bias is observed. For a positive bias, it is almost constant in contrast to Fig. 5.19 (a). For single fin devices presented in Fig. 5.20 (b), the mobility is almost the same over the whole bias range. Therefore, the trend of mobility for 5-fin 30 nm and 100 nm wide devices at negative PZT bias can be explained by the literature data.

The mobility dependency on the amount of fins could be related to the strain formed by the PZT layer along the surface between parallel fins. Each fin could form a kind of side clamping surface for the PZT layer in between parallel fins. The strain would then be more profound at the sidewalls of the middle 3-fins. Since PZT is biaxial tensile stressed after deposition, we expect a compressive stress along the fin width direction. This effect would be more profound in the narrow fin devices. In Fig. 5.18 (f), for a single fin device, the mobility is decreased more after deposition than in Fig. 5.17 (e), for a 5-fin device. This difference could be due an increased compressive stress along the fin width for a 5-fin device due to the clamping effect; which would result in turn in more tensile stress along the channel length direction.

In summary, a threshold voltage shift is observed after the piezoelectric layer deposition due to stress in the oxide and Si layers. A further shift is obtained under an applied bias over the piezoelectric layer, which is attributed to the leakage current induced surface potential change. The *SS* is also modified after deposition and under PZT bias. Change in the trap density due to oxide deformation could be a reason for this effect. Furthermore, a change in the electron mobility is observed after the PZT deposition. The low field mobility change could again be related to a change in effective trap density due to the stressed oxide layer. This change in mobility shows a fin width dependency also. Regarding the obtained device characteristics, PiezoFETs show a change in *SS* and mobility as a result of the presence of the piezoelectric layer.

5.4.4 *C-V* characterization

The capacitance-voltage (*C-V*) characteristics of the PiezoFETs can be used to study any degradation of the gate oxide properties after PZT deposition. *C-V* measurements were also done to measure the equivalent capacitance of the structure. Dedicated *C-V* test structures together with their open and short de-embedding pairs were designed as described in chapter 4. Each capacitance measurement was performed by de-embedding the contact pad as well as the parasitic connections. The capacitor dimensions are summarized in Table 5.2. The measurements were performed at V_{ac}= 20 mV and at 1 MHz frequency.

Fig. 5.21 shows the *C-V* curves obtained from parallel fin gate capacitors for 60 fins with W_{FIN}= 60 nm, L_{gate}= 20 µm, L_{pigate}= 4 µm. The capacitance values were calculated using Eq. (4.15). Since $\varepsilon_{\mathrm{PZT}}$ was determined to be 600 in chapter 3, the calculated PZT capacitance is 9.2×10^{-12} F and the calculated oxide capacitance is 1.36×10^{-12} F. Since the capacitances are in series, the equivalent capacitance equals 1.0×10^{-12} F. The calculated and measured capacitance values are presented in Table 5.4 showing good agreement. The relatively small difference between the calculated and measured equivalent capacitance could be due the voltage dependency of the dielectric constant of PZT which was not incorporated in the calculations.

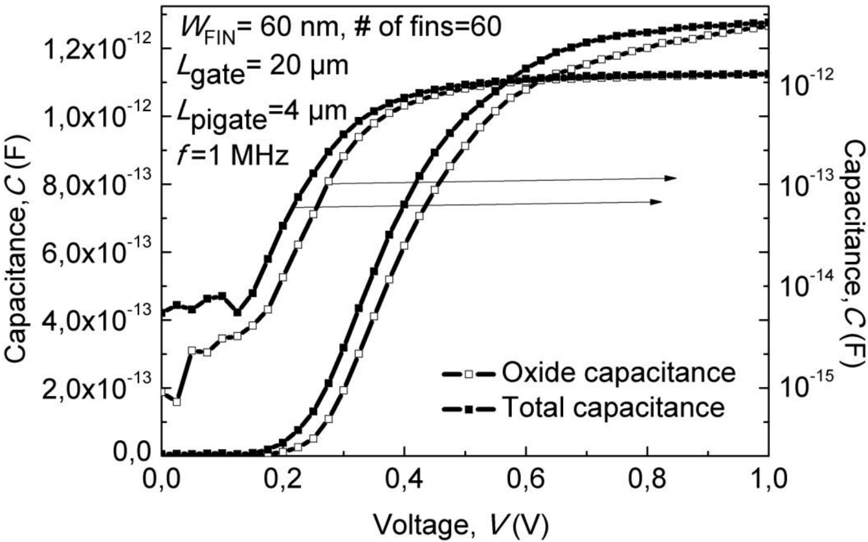


Fig. 5.21 *C-V* characteristics of the gate capacitor test structure containing 60 fins with W_{FIN}= 60 nm, L_{gate}= 20 µm, L_{pigate}= 4 µm. Measurements were performed at f = 1 MHz with V_{ac} = 20 mV.

Table 5.4 *Calculated and measured capacitance values for a parallel fin C-V test structure*

W_{FIN}= 60 nm, L_{gate}= 20 µm L_{pigate}= 4 µm	***Calculated***	***Measured***
Oxide capacitance of PiezoFET with 60 fins	1.36×10^{-12} F	1.28×10^{-12} F
Total capacitance of PiezoFET with 60 fins	1.00×10^{-12} F	1.25×10^{-12} F

This measurement is an indication that there is hardly any degradation in the properties of the oxide after PZT deposition. Furthermore, the *C-V* curve is also plotted in semi-log scale to investigate the trap related slope degradation. No serious change in the slope is observed, meaning that Si-oxide interface is not degraded due to PZT deposition. No further measurement data is presented with different area capacitors since the equivalent capacitance is close to that of the oxide capacitance.

The *C-V* measurement of the PZT layer on the channel was performed with dedicated test structures presented in Fig. 5.3. However, the relatively high leakage current (see e.g. Fig. 5.14) disturbed the measurements.

Bias temperature stress (BTS) measurements were also done to determine the amount of mobile charge concentration of the PiezoFET. The *C-V* test structures were used for these measurements. The experimental methodology used was as follows. During the measurement, the device was heated up to 150-200 °C and a gate bias was applied to produce an electric field in the order of MV/cm for 5-10 min causing mobile charge drifting to one interface. Then, the device was cooled down to room temperature under the applied field and a second *C-V* measurement is performed. The same procedure was repeated for the opposite field. The mobile charge can then be determined from the flatband voltage shift of the *C-V* curve [24].

Fig. 5.22 shows the *C-V* curves of the FinFET and PiezoFET before and after the BTS measurement. Before the BTS measurement, the capacitors were heated up to 200 °C and biased for 10 min under ±3 V ($E \approx \pm 2\text{x}10^5$ V/cm). Fig. 5.22 (a) shows the *C-V* measurements before PZT deposition. Figs. 5.22 (b) and (c) show the *C-V* measurements from bottom gate to channel and from top gate to channel, respectively.

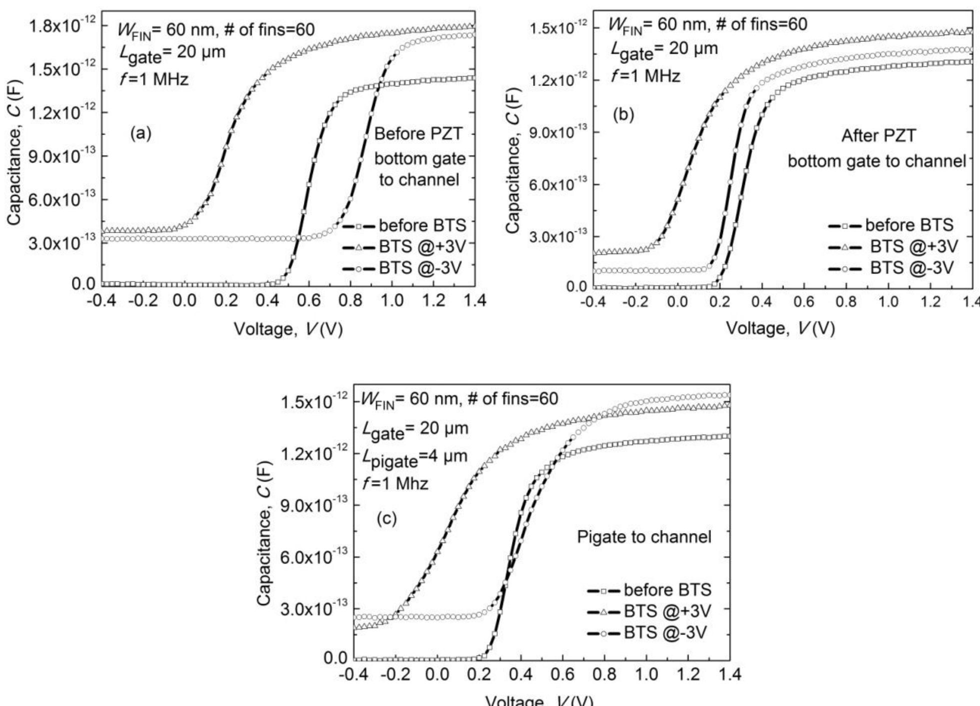


Fig. 5.22 C-V characteristics of the capacitor test structure with 60 fins and W_{FIN}= 60 nm, L_{gate}= 20 µm, L_{pigate}= 4 µm before and after the BTS (at 200 °C for 10 min) (a) before PZT deposition, (b) after PZT deposition, bottom gate to channel capacitance, (c) after PZT deposition, pigate to channel capacitance. Measurements were performed at f = 1 MHz with V_{ac} = 20 mV.

The general trend is that a relatively small negative shift has been observed in the threshold voltage after the capacitor has been stressed. The relatively small shift in threshold voltage is positive after stressing the capacitor at 200 °C for 10 min under -3 V bias. This shift has been observed before the PZT deposition also. This means that the gate oxide (SiO_2) layer contained already some mobile charge before PZT deposition and there is no sign of additional mobile charge due to the PZT layer. Since the threshold voltage shift is much smaller than the actual shift observed when biasing the PiezoFET, the mobile ions do not play a significant role in this effect. These mobile ions were possibly formed during the process of the FinFETs, hence before the PZT deposition. The results emphasize that PZT is compatible with FinFETs.

5.5 Conclusions

This chapter presents the processing and characterization of a novel four terminal device structure called the PiezoFET. The processing started by removing Al from the contact pads of the FinFETs. Afterwards, the PZT/LNO stack was deposited by PLD. Patterning of these layers was performed by wet etching and finally the Pt/Ti contact pads were

defined by a lift off process. For comparison, AlN deposited device characteristics have been presented as well.

Optical, physical, and ferroelectric characterization of the PZT layer was performed by XRD, LDV and *P-E* measurements. The piezoelectric activity of the PZT layer on the FinFETs was evidenced by its high d_{33} (≈100 pm/V) response, especially from the channel region.

The effect of the piezoelectric layer on the transport properties in the Si channel was studied by *I-V* measurements. No harmful effects were observed in device properties after piezoelectric layer deposition. A negative shift is observed in the I_d-V_{gs} curves after PZT and AlN deposition. This effect is related to the coefficient of thermal expansion (CTE) difference formed strain in the Si and the oxide. It causes a strong gate oxide deformation possibly affecting the band alignment and related charge trapping. The latter was supported by the observed change in the *SS*.

When the piezoelectric layer was biased at a constant field, a relatively high positive and negative ΔV_{th} was observed in the FinFET devices under high piezoelectric leakage current. An analogue electrical circuit is presented to explain this effect. The leakage paths are most probably created due to poor step coverage of the PZT and AlN layers around the fins. The extracted interface trap density shows a dependence on the PZT bias. By applying a bias over the PZT layer deforms the oxide layer and Si further which appears to change the amount of effective interface traps and hence *SS*.

The transport properties of the transistors were studied in terms of mobility. It is shown that the mobility at strong inversion decreases for 30 nm wide fin devices (stronger for a single fin device) whereas it increased (of up to ≈ 50 %) for 100 nm and 1000 nm wide fin devices after PZT deposition. An increase in the mobility after PZT deposition is again related to the strain formed by CTE difference. The same effect is also observed for AlN deposited devices. The type of strain in the narrow fins and wide fin devices are different. For a narrow fin, a compressive stress is formed along the channel length direction at the $(1\overline{1}0)$ surface of the fin sidewall, resulting in a lower mobility. For a wide fin device the stress is tensile at the (001) surface and the mobility increases accordingly.

Applying a bias over the PZT layer has also an effect on the mobility (up to ≈ 20 %), showing the converse piezoelectric effect. In the moderate inversion regime (near threshold voltage), the mobility decreases when the PZT layer is negatively biased. When the applied bias is positive, the 30 nm and 100 nm wide 5-fin devices show a higher mobility. This is related to an increased tensile stress along the channel length direction. A decrease of the mobility under negative bias, on the other hand, is related to an increased compressive stress along the channel length direction. Single fin devices show

hardly any effect in mobility. The strain effect is less in single fin devices possibly due to the absence of the fin sidewall clamping compared to multi-fin devices.

We obtain a less significant decrease in the effective mobility at the strong inversion mode of the 5-fin device when a negative bias is applied. However, when a positive bias is applied, the mobility is not affected. Furthermore, the mobility of a single fin device is almost constant over the whole bias range. The weak dependence of the mobility on the applied bias in strong inversion region is related to a quantization of carriers, which counteracts the stress induced repopulation of the electron valleys.

Furthermore, *C-V* measurements were performed to analyze any degradation in the oxide properties after PZT deposition. Almost no change has been observed in the *C-V* curves of the FinFETs after PZT deposition. BTS measurements were also performed to observe any effect due to mobile ions. No change is observed in the curves before and after PZT deposition. Therefore, there is no additional mobile charge related effects in the PiezoFET due to PZT layer.

With all these results, we conclude that PZT is successfully integrated with FinFETs and no harmful effects have been observed in the underlying device structure. In addition, despite the issues of the leakage current and poor step coverage, the measurements from different device configurations indicate a change in underlying device properties when the PZT layer is actuated.

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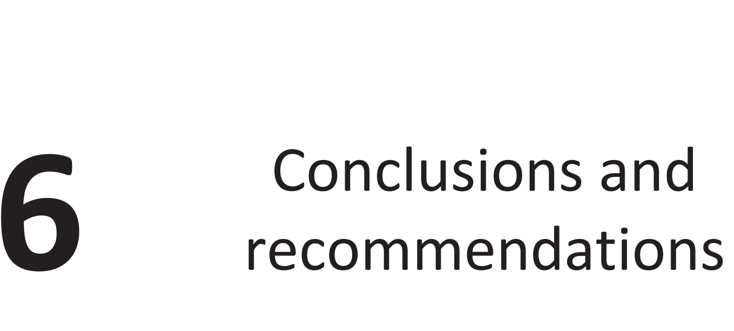
6
Conclusions and
recommendations

6.1 Conclusions

In this work, we investigated strained SOI FinFETs and the feasibility of usage and implementation of the converse piezoelectric effect as a stressor. Strain is often applied in semiconductor research and technology and in research projects to improve the device performance. We have studied the strain in FinFETs formed by the difference in coefficient of thermal expansion (CTE) of the thin film materials used. In addition, a next possible generation strained device structure, the PiezoFET, was realized and characterized. In this case, PZT was chosen as a stressor to obtain tunable strain due to its high piezoelectric constant.

I-V measurements were used to analyze the strain effects in the bandgap of $(1\bar{1}0)/[110]$ oriented n-type strained FinFETs obtained from NXP. Raman spectroscopy was also used to directly characterize the device level strain. An offset in conduction band energy down to ≈ -40 meV was determined from the electrical measurements. Depending on the dimensions of the fins, the effect of strain or strain including quantum confinement effects is present in the devices. Strain was formed due to a difference in CTE of TiN and Si. In addition, Raman spectroscopy measurements indicated a maximum of -0.88 % strain in the Si channel. Good agreement was obtained in strain values determined by Raman spectroscopy, FEM simulations and holographic interferometry. Therefore, Raman spectroscopy was shown to be a good method to obtain strain information from FinFET structures. Furthermore, the result obtained from the electrical analysis could be explained by using the strain-fin width relation obtained by these techniques.

Sub-100 nm thick thin-film PZT/LNO stacks on an encapsulated TiN electrode were studied to characterize their properties. A promising effective piezoelectric coefficient $d_{33,f}$ was obtained with a maximum of 53 pm/V for 75 and 100 nm thick films. Extensive analysis was done by capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements. The results indicate the presence of a passive layer at the electrode interface. A relative dielectric constant of the PZT layer of 600 was determined. The effective thickness and the relative dielectric constant of the passive layer was estimated to be 2.1 nm and 23, respectively. A lower than expected barrier height of 0.32 eV was obtained which is possibly caused by ferroelectric polarization induced barrier lowering. It was also shown that the leakage current can be described with a diffusion-based rather than a pure Schottky emission model.

In this study, FinFETs were designed, fabricated and characterized in MESA+. They serve as a base for our work on the PiezoFETs. The fabricated devices were analyzed by resistivity, *I-V* and *C-V* measurements. Devices with subthreshold swing (*SS*) of 76 mV/dec, a low leakage and high I_{on}/I_{off} (≈ 10^8) current were obtained. Good performance of our $(1\bar{1}0)/[110]$ oriented FinFETs was evidenced by these figures and by

comparison with the NXP-FinFETs characteristics with the same orientation. In addition, good effective mobility-electric field curve for long gate lengths (≈ 10 μm) were obtained in agreement with data from the literature.

Using these FinFETs as a base, PiezoFET devices were processed and characterized. No degradation was observed in the device characteristics after the piezoelectric layer deposition on the FinFETs. It is an indication of compatibility of PZT layer with Si device technology. The PZT capacitor showed a high piezoelectric response on the FinFETs, d_{33} ≈ 100 pm/V, especially from the channel region. I_d-V_{gs} measurements indicated a threshold voltage shift after PZT or AlN deposition without any bias. This shift appears to be related to the strain formed in the Si and in the oxide due to the difference in the CTE of Si and the covering layers. This strain deforms the relatively low stiff gate oxide and it can possibly affect the band alignment resulting in a change in effective interface trap density. The observed change in *SS* was a verification for the difference in trap charge density.

A relatively high positive and negative ΔV_{th} was observed under constant bias of the PZT piezoelectric layer. Furthermore, a high piezoelectric leakage current was observed in the same measurements due to poor step coverage of the piezoelectric layer. It was found that the leakage current through the piezoelectric layer and a comparable gate stack resistance resulted in a voltage drop over the bottom gate. As a result, the surface potential is increased by the voltage drop over the gate stack altering the V_{th}. Since single fin devices with a large fin width showed less leakage, we conclude that the leakage paths are mainly located at the fin sidewalls. This emphasizes the importance of the step coverage of the piezoelectric layer. Applying a bias over the PZT layer changed the *SS*. This could be due to further deformation of the gate oxide layer and Si, which results in a change of the effective interface trap density and hence *SS*.

The strong inversion mobility decreased for 30 nm wide fin devices whereas it increased (up to ≈ 60 %) for 100 nm and 1000 nm wide fin devices after PZT deposition. Strain in the channel and gate oxide formed by the difference in CTE could be a reason of an increase in the mobility. The same effect was also observed for devices with an AlN layer. The strain affects narrow fins and wide fin devices differently. For a narrow fin, the fin sidewall is more important and after deposition compressive stress is formed along the $(1\bar{1}0)$ fin sidewall, resulting in a lower mobility. For a wide fin, the (001) device surface is more important. In this case stress is tensile at the (001) surface and the mobility increases accordingly.

Biasing the PZT layer changed the mobility up to ≈ 20 %. This is an indication of the converse piezoelectric effect. When the PZT layer was negatively biased, we observed a decrease in mobility in the moderate inversion regime. When the applied bias was

positive, a higher mobility was observed for 30 nm and 100 nm wide 5-fin devices. This indicates an increase in tensile stress along the channel length direction. When the applied bias was negative, mobility decreased. This could be an indication of an increase in compressive stress along the channel length direction.

Furthermore, the *C-V* curves of the gate capacitor before and after deposition of the piezoelectric layer were almost the same. Bias temperature stress measurements were also performed and again no change was observed in the curves before and after PZT deposition. Therefore, we conclude that there is no additional mobile charge related effects in the PiezoFET induced by the PZT layer.

The fabricated PiezoFET is a good candidate for several applications. There is a possibility to obtain a lower *SS* than the base transistor using a piezoelectric layer. The *SS* of a device can also be controlled up to certain limits. Therefore, it can be used as an alternative FET design. Furthermore, the higher effective mobility compared to its base FinFETs makes it a candidate as a replacement of the FinFET. In addition, due to the large shifts in V_{th} values, it can be applied as a memory with a large memory window of about 3 V. Such a memory device based on the leakage current has been patented before [1]. Since this memory device does rely on a ferroelectric hysteresis effect, the memory window is more stable than FeRAMs.

6.2 Recommendations

The converse piezoelectric effect formed strain concept is a good candidate to obtain steep sub-threshold devices. Our results have demonstrated the feasibility and great potential of the concept. However, considering our results, there are several points that can be improved.

Since the converse piezoelectric effect relies on the mechanical displacement, it is important to keep the interlayer thicknesses as small as possible. The thickness of LNO as a PZT buffer layer cannot be decreased further since, as shown in chapter 3, the growth properties of PZT show high dependence on this layer thickness. However, the thickness of the underlying layers can be decreased for this purpose. Replacing the SiO_2 layer of 11 nm thickness by a high-κ HfO_2/SiO_2 layer of 2-3 nm thickness could be one way. In addition, the thickness of 12 nm α-Si encapsulating layer can be decreased down to ≈ 5 nm; below which the film is not continuous. In this way the stress in the channel can be improved.

The step coverage of the piezoelectric layer is very important. The leakage paths are easily formed when the layer is thinner on the sidewalls. This leakage current forms a voltage drop on the bottom gate. A better step coverage will result in an improved

structure for electrical characterization and analysis of the PiezoFET concept. CVD or ALD techniques could be used to obtain good step coverage. Although ALD is not obvious for the PZT deposition, it can be used for AlN deposition. Preventing leakage will also help to understand the strain modulation effect on the device transport properties.

Since the FinFET/PiezoFET is a 3D device structure, strain components from the top and the sidewall have to be taken into account. In addition, the fin height needs to be optimized in the range of thickness of the piezoelectric layer to control the strain in the Si channels. Therefore, although higher strain values can be obtained using 3D narrow channels, there are some complications in understanding and calculating the individual components. Piezoelectric layers on planar surfaces, on the other hand, form a more uniform strain distribution in the Si channel. For this reason, using planar structures can be a good alternative for an extensive study on the PiezoFET device concept.

Reference

[1] I. K. Yoo, "Ferroelectric Memory Using Leakage Current and Multi Numeration System Ferroelectric Memory", United States Patent, Patent No 5,812,442, 1998.

Summary

Strain is often applied in semiconductor technology to improve the device performance in a field effect transistor (FET). However, it increases the off-state current as well. In this work, we investigated so-called silicon-on-insulator (SOI) fin-shaped field-effect transistors (FinFETs) and the effects of strain formed by the difference in coefficient of thermal expansion (CTE) of the used materials. Near ideal SOI FinFETs were realized in the clean room of MESA+ Institute for Nanotechnology. They served as a base for our new strained device structure: the PiezoFET. The PiezoFET is a novel device in which the channel strain can be controlled by a piezoelectric stressor to keep the off-current the same while increasing the on-current. In this device structure, PZT was used as a stressor and the effects of strain modulation due to the converse piezoelectric (piezo) effect in these devices were shown.

Chapter 1 presents the motivation, the project description and the objectives. Concepts of steep sub-threshold devices reported from literature are summarized and the effects of strain in Si channels are addressed. The reasoning behind the preferred device configuration, the SOI FinFET, and the use of TiN as a bottom gate are discussed. A new device concept, called the PiezoFET, is introduced. In this device the converse piezoelectric effect from PZT is used to induce strain modulation in the Si channels.

In chapter 2 electrical analysis and Raman spectroscopy were used to study device level strain in (110) oriented n-type Si strained FinFETs. In these devices strain was formed by the difference in CTE of the Si fin and the TiN gate material. An offset in conduction band energy down to ≈-40 meV was determined from the electrical measurements. This offset is changing depending on the fin dimensions. It can be explained by counteracting quantum confinement and strain effects. Raman spectroscopy measurements indicated a maximum of -0.88 % strain in the Si channel. The strain values obtained from Raman measurements, FEM simulations and holographic interferometry are in good agreement. Raman spectroscopy was shown to be a good method to obtain actual strain values in

FinFET structures with nanometer dimensions. In addition, electrical measurement results could be explained by the picture drawn by these techniques.

In chapter 3 a brief introduction to ferroelectrics films and applications is given. Next the properties of thin PZT films used in the PiezoFET were investigated. A promising effective piezoelectric coefficient $d_{33,f}$ was obtained with a maximum of 53 pm/V for 75 and 100 nm thick films. Extensive analysis was done by capacitance-voltage (*C-V*) and current-voltage (*I-V)* measurements. The results indicate the presence of a passive layer at the electrode interface. A relative dielectric constant of the PZT layer of 600 was determined. The effective thickness and the relative dielectric constant of the passive layer was estimated to be 2.1 nm and 23, respectively. A lower than expected barrier height of 0.32 eV was obtained which is possibly caused by ferroelectric polarization induced barrier lowering. A good fit of the measurement data with theory revealed that leakage current can be described by a diffusion-based rather than a pure Schottky emission model.

In chapter 4 our FinFETs are described. These devices were designed and fabricated in the clean room of the MESA+ Institute for Nanotechnology. They were analyzed by resistivity, *I-V* and *C-V* measurements. Results revealed a near-ideal behavior of the FinFETs with a sub-threshold swing (*SS*) of 75 mV/dec, a low leakage and high I_{on} / I_{off} (≈ 10^8) ratio. The performance of our FinFETs was comparable with the NXP-FinFETs characteristics described in chapter 2. In addition, the effective mobility-electric field curves for long gate lengths (≈ 10 µm) were in agreement with data from the literature. These FinFETs served as the base for our work on the PiezoFETs described in chapter 5.

In chapter 5 the processing and characterization of the PiezoFETs are presented. After the PZT deposition no harmful effects were observed in the underlying device characteristics. In the I_d-V_{gs} measurements a shift in threshold voltage was found. This shift is partly due to the strain formed in the Si channel by the difference in the CTE of Si and the layers on top. This strain also deforms the gate oxide resulting in a change in the effective trap density at the Si-gate oxide interface. This resulted in the observed change in the *SS* in our PiezoFETs.

The PZT capacitors in the PiezoFET devices showed a high piezoelectric response, d_{33} ≈100 pm/V, especially from the channel region. Biasing the PZT layer indicated the action of the converse piezoelectric effect. It changed both the *SS* and the electron mobility. The change in *SS* could be due to a further deformation of the gate oxide layer and the Si, resulting in a change of the effective interface trap density and hence the *SS*. Also a change in the mobility up to ≈20 % was measured. For low V_{gs} this is can be explained again by the change of the effective interface trap density; since then Coulomb scattering is important. However, for high $V_{gs,}$ this is more related to stress in the Si. When the

applied bias was positive, a higher mobility was observed for 30 nm and 100 nm wide 5-fin devices. This indicated an increase in tensile stress along the channel length direction. On the other hand, when the PZT layer was negatively biased, a decrease in mobility was found due to an increase in compressive stress along the channel length direction.

The fabricated PiezoFET device is a good candidate for several future applications. Due to the possibility to obtain a lower and controllable *SS* compared to the base transistors, it can be an alternative FET design. The higher effective mobility makes it a reference point for improvement of the FinFET characteristics.

Samenvatting

Mechanische vervorming (*strain*) wordt in de halfgeleider technologie vaak toegepast om de prestaties van een veld-effect transistor (FET) te verbeteren. Het kan echter ook de uit-stroom verhogen. In dit werk hebben we de zogenaamde silicium op isolator (SOI) vinvormige (fin) veld-effect transistoren (FinFETs) onderzocht en de effecten van strain in de silicium (Si) vin. Deze strain kan worden gevormd door het verschil in thermische uitzettingscoëfficiënt van de gebruikte materialen. Zeer goede SOI FinFETs zijn in de stofarme ruimte van het MESA+ Instituut voor Nanotechnologie gemaakt. Zij dienden als basis voor onze nieuwe vervormbare structuur: de PiëzoFET. De PiëzoFET is een structuur waarin door middel van een piëzo-elektrisch materiaal vervorming in de vin kan worden bewerkstelligd, zodanig dat de uit-stroom hetzelfde blijft terwijl de aan-stroom verhoogd wordt. In deze structuur werd lood zirconaat titanaat (PZT) gebruikt als piëzo-elektrisch materiaal. De effecten als gevolg van de piëzo-elektrische werking in deze FinFET structuren werden aangetoond.

Hoofdstuk 1 geeft de motivatie, de beschrijving van het project en de opzet. Voorbeelden van elektronische elementen met steile sub-drempelstroom (steep sub-threshold devices) uit de vakliteratuur zijn samengevat en de effecten van de mechanische vervorming op het Si worden behandeld. De keuze van de SOI FinFET structuur en de toepassing van titanium nitride (TiN) als electrode wordt toegelicht. Een nieuw ontwerp, de zogenaamde PiëzoFET, wordt geïntroduceerd. Hierin wordt het inverse piëzo-elektrische effect van PZT gebruikt om strain in het Si te bewerkstelligen.

In hoofdstuk 2 worden elektrische metingen en Raman spectroscopiemetingen gebruikt om de strain in (110)-georiënteerd n-type Si vinnen in FinFETs te bestuderen. In deze structuren werd de strain veroorzaakt door het verschil in thermische uitzettingscoëfficiënten van het Si en het TiN electrode materiaal. Uit de elektrische metingen werd een verschuiving van de energie van de geleidingsband van ≈-40 meV bepaald. Deze verschuiving was afhankelijk van de afmetingen van de vinvormige

structuren. Dit kon worden verklaard uit de wisselwerking van kwantumopsluiting en de effecten van strain in het Si. De Raman spectroscopiemetingen toonden een maximale strain van de Si vin van -0.88%. De waarden uit de Raman spectroscopiemetingen, eindige-elementen (FEM) simulaties en holografische interferometrie kwamen goed overeen. Raman spectroscopie bleek een goede methode om de werkelijke strain in Si FinFETs te bepalen.

In hoofdstuk 3 wordt allereerst een korte inleiding gegeven over ferro-elektrische lagen en de toepassingen daarvan. Daarna werden de eigenschappen van dunne PZT lagen voor de PiëzoFET onderzocht. We vonden een veelbelovende maximale effectieve piëzo-elektrische coëfficiënt van 53 pm/V voor 75 en 100 nm gedimensioneerde PZT lagen. Een uitgebreide analyse aan de hand van capaciteit-spanning (*C*-*V*) en stroom-spanning (*I*-*V*) metingen werd uitgevoerd. De resultaten wezen op de aanwezigheid van een passieve laag bij het grensvlak met een elektrode. De effectieve dikte van deze laag werd geschat op 2,1 nm met een diëlektrische constante van 23. De verkregen barrièrehoogte van 0,32 eV was lager dan verwacht. Dit wordt mogelijk veroorzaakt door ferro-elektrische polarisatie. Een goede overeenkomst van de meetgegevens met de theorie voor de lekstroom wijst op een model gebaseerd op diffusie boven dat van zuivere Schottky emissie.

In hoofdstuk 4 worden onze FinFETs beschreven. Deze structuren werden ontworpen en ze werden gemaakt in de stofarme ruimte van het MESA+ Instituut voor Nanotechnologie. De analyse bestond uit weerstands-, (*I*-*V*)- en (*C*-*V*) metingen. De resultaten lieten zeer goede eigenschappen van de FinFETs zien met een sub-drempel zwaai (sub-threshold swing) *SS* van 75 mV/dec, een lage lekstroom en een grote verhouding van de aan- en uit-stroom (I_{on}/I_{off}) ≈ 10^8. De prestaties van onze FinFETs was vergelijkbaar met de FinFETs van NXP zoals beschreven in hoofdstuk 2. Bovendien was er een goede overeenstemming tussen de gemeten verbanden van de effectieve mobiliteit en het aangelegde elektrische veld voor lange Si vinnen (≈ 10 μm) en de gegevens uit de vakliteratuur. Deze FinFETs dienden als basis voor het werk aan PiëzoFETs zoals beschreven in hoofdstuk 5.

In hoofdstuk 5 worden het maken en de karakterisering van de PiëzoFETs gegeven. Na het aanbrengen van de PZT laag werden er geen schadelijke gevolgen in de onderliggende Si vinstructuren waargenomen. In de I_d-V_{gs} metingen werd een verschuiving van de drempelspanning gevonden. Deze verschuiving is gedeeltelijk toe te schrijven aan de strain in het Si door het verschil in thermische uitzettingscoëfficiënten van het Si en de lagen erboven. Dit vervormt ook het poortoxide (SiO_2) van de FET, wat een verandering in de dichtheid van de effectieve elektrische defecten (traps) aan het grensvlak van het Si en het SiO_2. Dit verklaart de waargenomen verandering in de PiëzoFET.

De capaciteiten van PZT in de PiëzoFETs lieten een grote piëzo-elektrische respons van ≈100 pm/V zien, in het bijzonder in de gebieden met de Si vinnen. Hier liet een elektrische voorspanning op de PZT laag de werking van het inverse piëzo-elektrische effect zien. Het veranderde zowel de *SS* als de elektronen mobiliteit. De verandering in *SS* wordt mogelijk veroorzaakt door een verdere vervorming van het Si en het SiO_2. Dit verandert de dichtheid van de effectieve traps aan het grensvlak en ook de *SS*. Er werd ook een verandering van de mobiliteit tot ≈20 % gemeten. Voor een lage V_{gs} kan dit weer verklaard worden door een verandering in de dichtheid van effectieve traps, omdat dan Coulomb verstrooiïng belangrijk is. Echter, voor hogere V_{gs} is dit meer direct gekoppeld aan de strain in het Si. Als de voorspanning posifief was, werd in structuren van 5 vinnen van 30 en 100 nm breed een hogere mobiliteit gevonden. Dit wijst op een toename van de mechanische trekspanning in de lengterichting van de vinnen. Anderzijds, voor een negatieve voorspanning werd er een lagere mobiliteit gevonden, dit als gevolg van een mechanische drukspanning in de lengterichting van de vinnen.

De onderzochte PiëzoFET is een goede kandidaat voor verscheidene toekomstige toepassingen. Door de verkregen lagere en instelbare *SS*, vergeleken met de oorspronkelijke transistor, kan deze structuur gebruikt worden als een alternatief ontwerp van een FET. De hogere mobiliteit vormt een goed uitgangspunt voor de verbetering van FinFETs.

List of publications

Journal Papers

- **B. Kaleli** , R.J.E. Hueting, M.D. Nguyen, R.A.M. Wolters, "*Integration of a piezoelectric layer on Si FinFETs for tunable strained device applications*", submitted to IEEE Transactions on Electron devices.

- **B. Kaleli**, M.D. Nguyen, J. Schmitz, R.A.M. Wolters, R.J.E. Hueting., *"Analysis of ferroelectric and electrical properties of sub-100 nm thick PZT/LNO stacks on an encapsulated TiN electrode"* submitted to Microelectronic Engineering.

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